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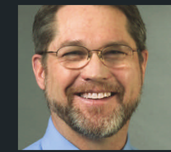

DISPLAYPORT VERSUS HDMI:
Do we really need two digital-display-interface standards?

Page 38

SILICON GERMANIUM:
FAST, QUIET, AND POWERFUL

Page 27

MAKING THE TRANSITION FROM BIT BANGER TO GIGABIT GURU

Page 47

System-Level ESD Protection Devices

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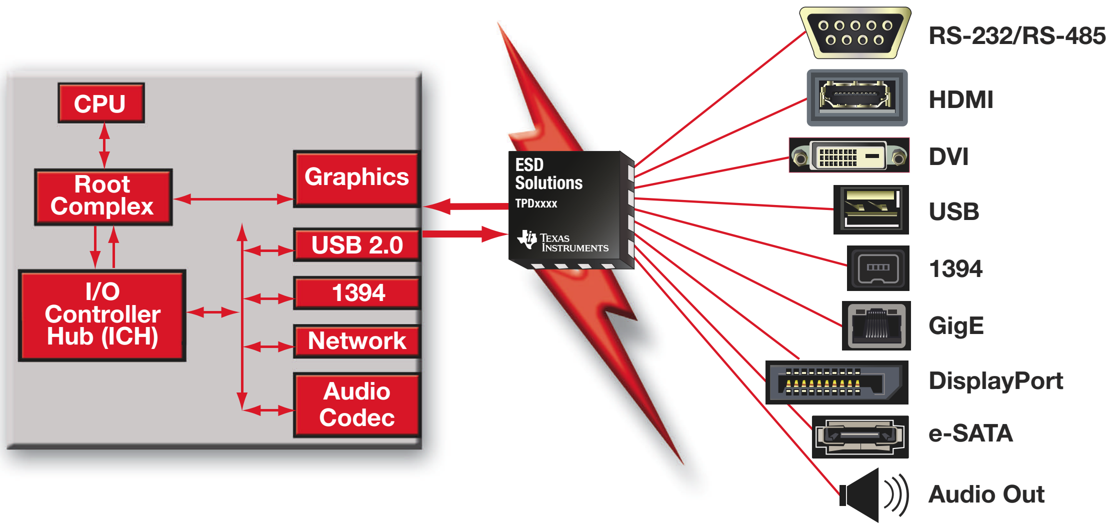

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TPD4E001	4	0.9-5.5	0-V_{DD}	1.5	11	SOT-6, SON-6	USB 2.0, Ethernet, Firewire, e-SATA, RS-232 / RS-485
TPD6E001	6	0.9-5.5	0-V_{DD}	1.5	11	QFN-10, QFN-12	USB 2.0, Ethernet, Firewire, e-SATA, RS-232 / RS-485
TPD4E004	4	0.9-5.5	0-V_{DD}	1.6	6	SOT-6, SON-6	USB 2.0, Ethernet, Firewire, e-SATA
TPD6E004	6	0.9-5.5	0-V_{DD}	1.6	6	QFN-8	USB 2.0, Ethernet, Firewire, e-SATA
TPD4S009	4	0.9-5.5	0-V_{DD}	0.9	9	SOT23-6, SC70-6, SON-6	e-SATA, LVDS signaling
TPD8S009	8	0.9-5.5	0-V_{DD}	0.9	9	SON-15	HDMI, DisplayPort
TPD12S520	12	0.9-5.5	0-V_{DD}	0.9	9	TSSOP-38	HDMI receiver port
TPD12S521	12	0.9-5.5	0-V_{DD}	0.9	9	TSSOP-38	HDMI transmit port

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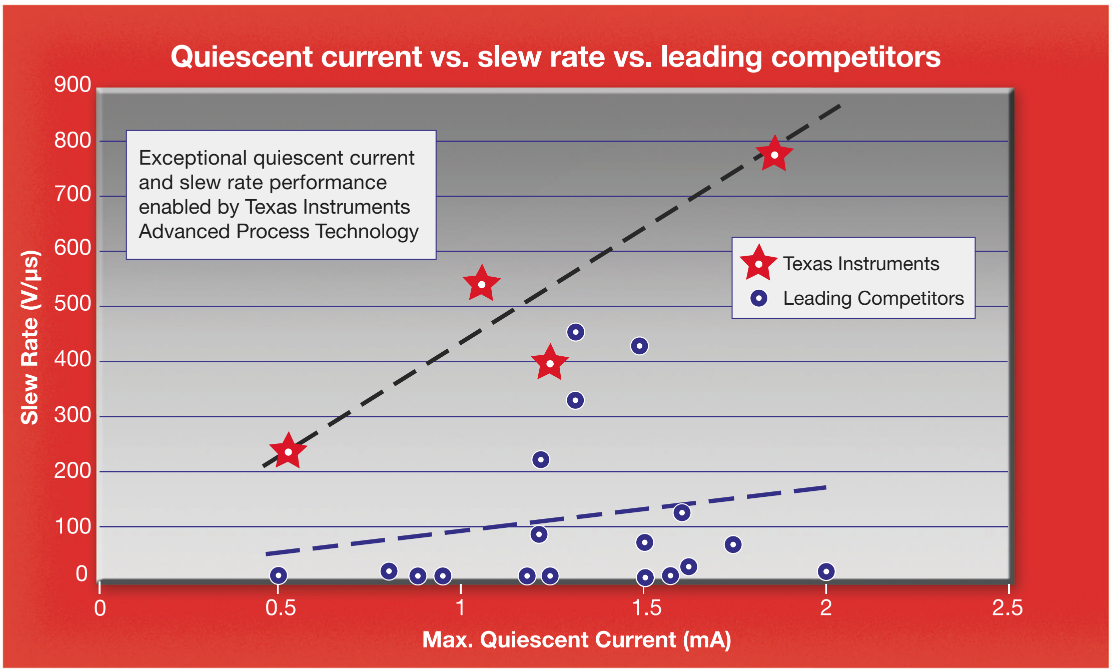

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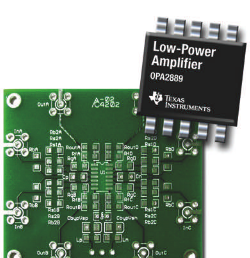

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EDN contents

9.18.08

Making the transition from bit banger to gigabit guru

47 As high-speed serial interconnections infiltrate technology, system designers face a series of new signal-integrity problems to manage. *by Eric Bogatin, PhD, Bogatin Enterprises, and Bill Hargin, Mentor Graphics*

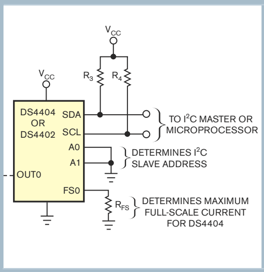
DisplayPort versus HDMI: Do we really need two digital-display-interface standards?

38 DisplayPort silicon is beginning to appear in PCs, LCD monitors, and graphics cards. But it will probably be at least five years before prices fall and volumes ramp enough to challenge HDMI in consumer electronics. *by Ann R Thryft, Contributing Technical Editor*

Silicon germanium: fast, quiet, and powerful

27 SiGe processes can give analog-circuit designers fast, high-voltage transistors with lownoise, whereas BiCMOS SiGe fits into CMOS-process flows. *by Paul Rako, Technical Editor*

DESIGNIDEAS



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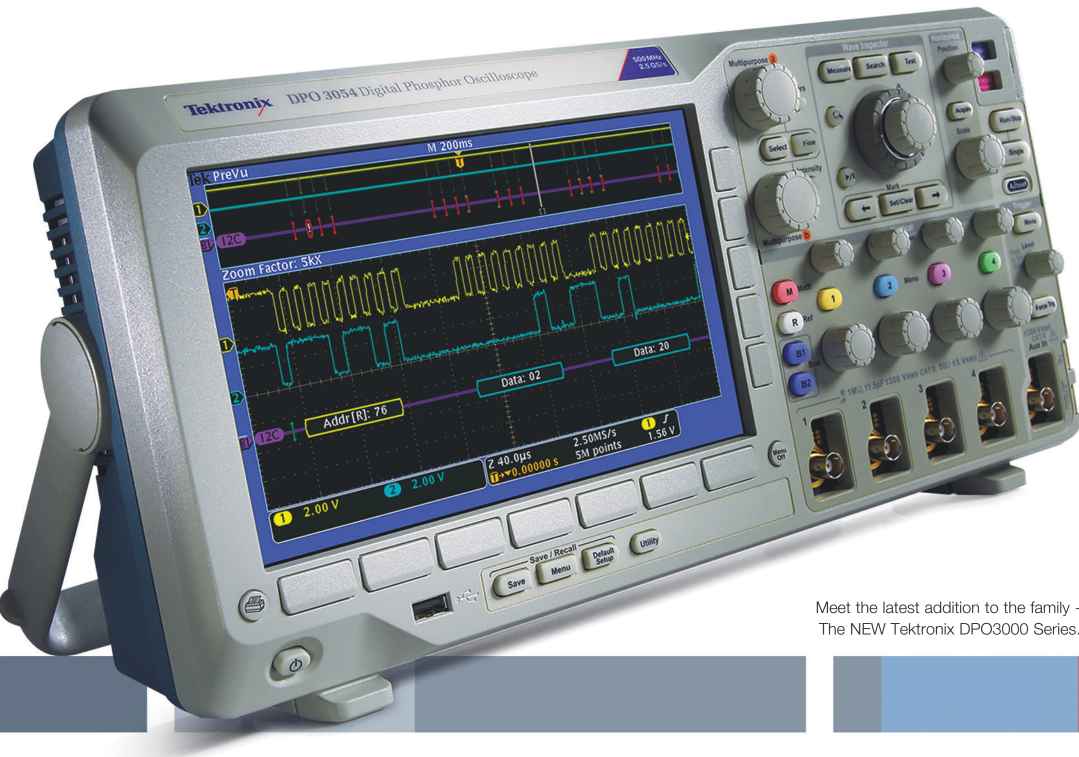

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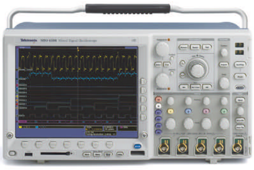

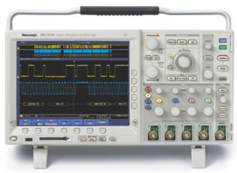

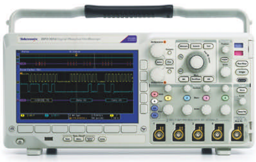

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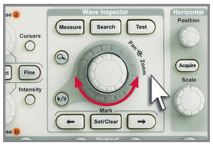

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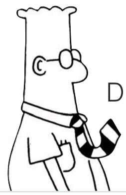

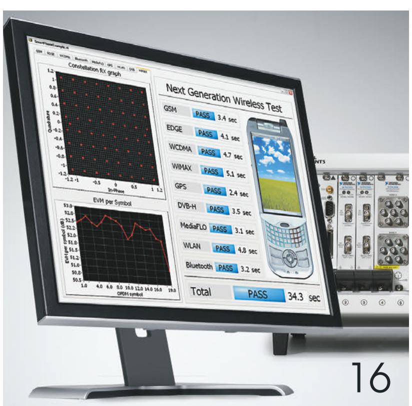

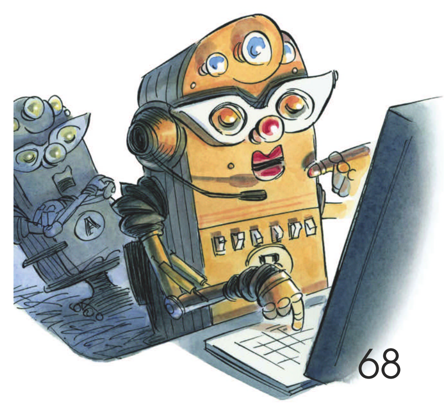

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BY BRIAN DIPERT, SENIOR TECHNICAL EDITOR

The turn of Apple's worm: Success accelerates its stumbles

When the news of Apple's move to Intel became official three-plus years ago, I remember that two sequential thoughts rapidly flew through my head: (1) Wow, this is going to really improve Apple's hardware competitiveness (cost, performance, and power consumption), translating to some impressive market-share growth over the next few years when coupled with the security vulnerabilities of competitor Microsoft's Windows XP, and (2) Wow, Apple's in trouble. The higher they climb, the harder they tend to fall.

I realize that these two statements are seemingly contradictory. I've followed Apple to one degree or another through my *EDN* career (more so in recent times). Before that, I also interacted with the company in my role as an applications engineer and manager with Intel's flash-memory group. My consistent impression of Apple, which others have also documented over the years, is one of a company immersed in a culture of control and secrecy. The origins of this culture can be traced to Chief Executive Officer Steve Jobs.

Apple's historically tight grasp on hardware, operating system, and applications suites, these suites often to the exclusion of third-party "partners" (just ask Adobe, for example), has led to a comparatively stable computing platform as compared with the Windows alternative. But the resultant dearth of hardware, software, and peripheral options (again, versus Windows) has also historically acted as a market-share cap. Now, however, a critical mass of consumers are fed

Apple is targeting a much larger market of Windows converts, who expect Windows-reminiscent ecosystem diversity.

up with Windows. Apple hardware is speedier, "battery-stingier," and more price-friendly than it's ever been, thereby creating a "perfect storm" for the company—but one that'll capsize it if it's not careful.

Paranoia was perhaps acceptable when Apple sold its products to only a few-market-share-percentage points' worth of perennial loyalists. Now, however, Apple is targeting a much larger market of Windows converts, who expect Windows-reminiscent ecosystem diversity. These converts also expect a more stable software experience than could be found in their Windows past, but they don't realize that the two aspirations are mutually exclusive.

I own almost as much OS X-powered hardware as I do Windows-based gear, so I feel qualified to comment that the blizzard of regularly appearing Apple-operating-system and -application patches is at least as heavy as that on the Windows side of the house, if not more so. And just as with Windows, Apple-offered updates regularly go awry, get pulled (but not in time for early adopters, who end up with DOA hardware as a result), patched, and reposted.

As the OS X ecosystem expands, Apple will out of necessity rely increasingly on peripheral drivers and other code supplied by third parties—third-party code that is at the core of most of the Windows stumbles that users regularly and incorrectly blame on Microsoft. And to that point, hypocrisy is at the root of my early-August DNS (Doman Name System) diatribe (see the original post at www.edn.com/080918ed1). Apple's TV commercials, for example, gloatingly make fun of Windows' "blue screen of death," security shortcomings, and other issues. Yet, based on early indications in this era of the iPod halo effect, I see no evidence that Apple will do any better in this regard; if anything, I'll wager that the converse will be the case. EDN

Contact me at bdipert@edn.com.

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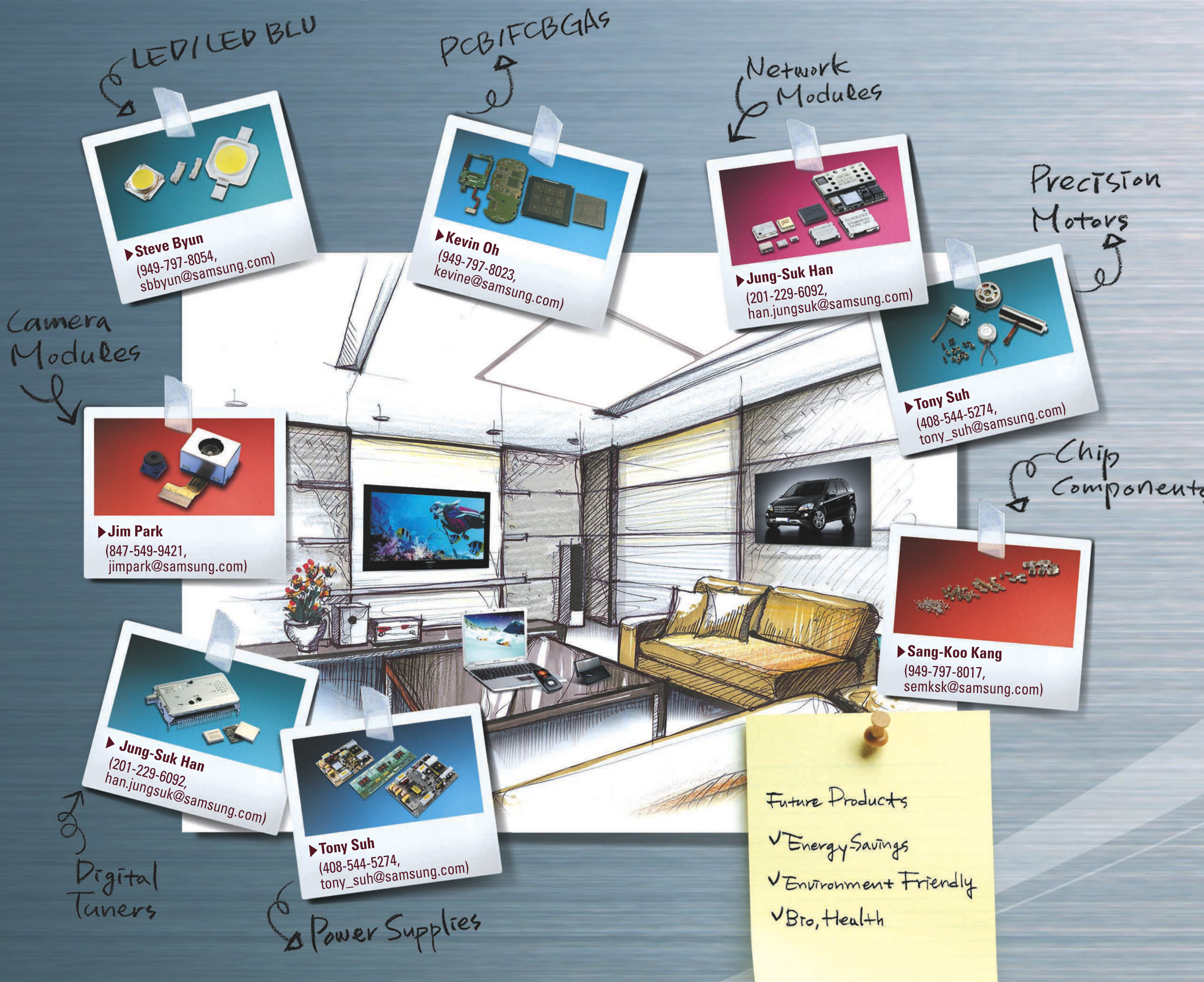

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DESIGN BRIEF

Battery-Charger Front-End IC Improves Charging-System Safety

By Mao Ye
Applications Engineer, Battery Management Applications

Introduction

Many types of adapters are available to charge the lithium-ion (Li-ion) battery and power the system, and their electrical specifications usually differ from one manufacturer to another. This challenges system designers to build portable devices that will meet safety and reliability requirements when used with different adapters. This article describes a new battery-charger front-end (CFE) IC, the Texas Instruments (TI) bq243xx, which is optimized to improve the safety of charging Li-ion-powered systems. Together with the battery-charger IC and the protection module in a battery pack, a charging system using the bq243xx CFE provides more robust system-level protection.

Main Safety Concerns in Charging Systems

Damage to the charging system can occur due to input overvoltage, input overcurrent, battery overvoltage, or reverse input voltage.

Input overvoltage can be caused by hot-plugging an adapter or using the wrong adapter; or by a transient or steady-state overvoltage condition. The most common occurrences are from hot plugging a charged, unregulated, or incorrect adapter; or from load transients. The unregulated adapter under no load will charge the adapter's output capacitor to the peak rectified AC voltage, about 1.4 times the rated DC voltage. This is often an issue with "low-voltage-process" (7-V-process) ICs. Figure 1 shows the output voltage of a typical regulated adapter versus an unregulated adapter.

Input-overcurrent challenges are not an issue with stand-alone chargers, since their constant-current mode limits the amount of current delivered to the output or battery. However, with power-path-management parts, which have a direct connection from the input to the system bus voltage, there is often no protection from excessive current draw. Lately there has been some concern over the safety of operating adapters in their current-limit mode and a desire for a programmable input-current-limit circuit to ensure that the adapter does not get into this mode.

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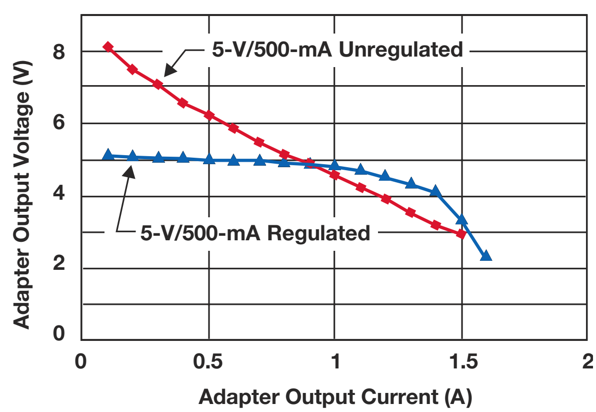

Figure 1. Regulated- and unregulated-adapter load lines.

Texas Instruments

Li-ion and Li-polymer battery packs are known for the potentially dangerous "flaming" condition that can occur if they are overcharged under high temperature. The key indication of overcharging is excessive cell voltage. To improve battery safety, many manufacturers are adding second-level overvoltage protection to remove the input power source when battery overvoltage is detected.

With universal connectors, it is a concern that an adapter with reverse polarity will be connected to the input. Without input reverse-polarity protection, the parasitic diode between the substrate and the IC will become forward-biased, causing a malfunction or damage to the IC.

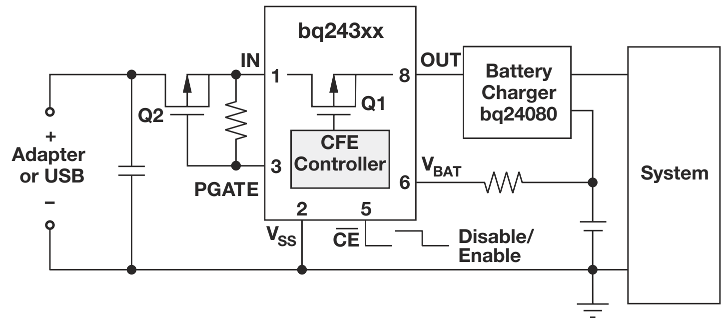

Figure 2. Typical PWM waveforms.

CFE Solution for Improving Battery-Charger Safety

Figure 2 shows a typical circuit for a battery-charging system with a bq243xx CFE. The CFE protects the system from input overvoltage by isolating high input voltage from the low-voltage charger and system. The bq243xx family offers a soft-start function to avoid inrush current and can provide input-current regulation and protection, output-voltage limiting/regulation, or battery overvoltage protection. Also available are optional features such as PGATE to drive an external FET for reverse-polarity protection; fault-status indication; a programmable input-current limit; and enable/disable input power.

Figure 3 shows the typical response of the bq24314 CFE to input overvoltage. The internal MOSFET switch immediately turns off with less than a 1-μs delay once the input voltage reaches the predetermined input-overvoltage threshold.

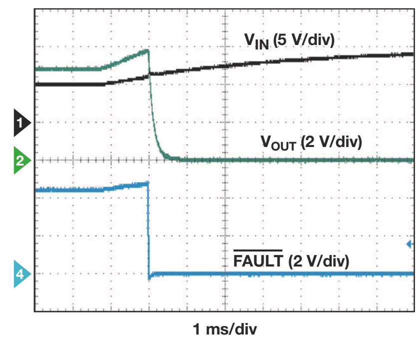

Figure 3. Protective response of bq24314 to input overvoltage.

When the system load exceeds the input-current limit, the CFE activates the input-current regulation loop and provides the maximum current limit set by the CFE. At a certain overcurrent blanking time, the CFE will turn off the MOSFET and may enter hiccup mode or latch mode after overcurrent protection is activated 15 times, depending on the IC version. The typical hiccup and latch response of the bq24314 CFE to input overcurrent is shown in Figure 4.

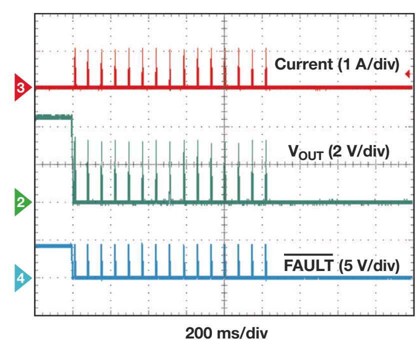

Figure 4. Protective response of bq24314 to input overcurrent.

Another key function of the CFE is to achieve battery second-level overvoltage protection for improved safety, although the battery pack itself achieves cell overvoltage protection by turning off the protection MOSFET in series with the cell. When the battery is overcharged due to any failure of the battery charger or protection MOSFET, the CFE will turn off its output with a 176-μs delay time and will recover when the battery is no longer experiencing overvoltage.

Please see Reference 1 for the complete version of this article, which includes more information about reverse-polarity protection and protective-response waveforms for the bq24314 with battery overvoltage.

Summary

The CFE can significantly improve the safety of battery-operated systems by fully integrating protection from input overvoltage, input overcurrent, battery overvoltage, and reverse input polarity.

Reference

1. View the complete article at http://www-s.ti.com/sc/techlit/slyt294

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INNOVATIONS & INNOVATORS

External power adapter combines USB power with interchangeable ac plugs

Portable consumer products increasingly rely on the USB port as a dc-power port. The ubiquitous port obviates the need for designers to use that annoying external-power-supply "wall wart" to charge a device's internal battery or directly power the device. Perhaps more important, because the USB port is an international standard, applications need provide only one power connection to satisfy international markets. The 8W PSM08R adapter from Phihong has a micro-USB output connector and is available with four interchangeable clip-adapter plugs for use in virtually any power outlet worldwide, allowing the use of a single power-adapter part number and simplifying a design's BOM (bill-of-materials) costs.

Phihong's 8W PSM08R adapter has a micro-USB output connector and is available with four interchangeable clip-adapter plugs for use in virtually any power outlet worldwide.

The double-insulated adapter has an ac-input range of 90 to 264V and an output of 1.6A at 5V dc and provides short-circuit and overvoltage protection. It meets the Energy Star IV specification and fully complies with the US Energy Independence and Security Act. The PSM08R sells for $13.06 (10); the adapters are priced separately.

—by Margery Conner

▷**Phihong**, www.phihong.com.

FEEDBACK LOOP

"I don't think we are going to be able to find the 'natural' state again, much less restore things to it. That doesn't mean we are stupid with our environment, but it also doesn't mean we run from our ability to manage it."

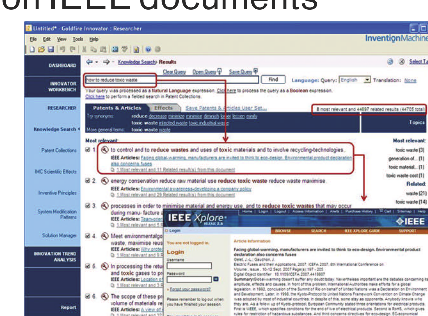
—Reader Dave Maples, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6578152. Add your comments.

Innovation-aid software gets infusion of 1.3 million IEEE documents

Invention Machine has announced the addition of 1.3 million technical documents from the IEEE (Institute of Electrical and Electronics Engineers) to its Goldfire Innovator software tool, which helps engineers and manufacturers generate and research product-development ideas. The collaboration ties the IEEE's Xplore digital library to Goldfire Innovator's knowledge base, which will automatically receive updates of new content. Goldfire users will be able to discover IEEE technical documents, including journal articles and conference proceedings, as part of the software's "concept-retrieval" process. To access the full text, users must be IEEE members, subscribe to Xplore, or purchase articles à la carte.

Invention Machine claims that Goldfire accelerates innovation by enabling companies to use natural-language queries to discover both internal and external information, which it organizes using a patented semantic engine. The tool allows companies to express both problems and opportunities in a common language and then helps them access precise information to help generate and validate ideas and analyze trends, such as patent activity.**—by Matthew Miller**

▷**Invention Machine**, www.invention-machine.com.



The Goldfire Innovator software tool, which now has access to 1.3 million technical documents from IEEE, accelerates innovation by enabling companies to use natural-language queries to discover both internal and external information.

LabView 8.6 adds wireless, enhances multicore and FPGA features

> The software lets you convert LabView applications into Web services.

National Instruments continues to expand the horizons for LabView, its popular graphical programming language. With the introduction of Version 8.6, LabView can now control the company's wireless data-acquisition products, and the software also extends beyond its traditional test-and-measurement base into multicore processing and embedded-system design. LabView 8.6 lets you make remote measurements using a Wi-Fi connection to data-acquisition devices. You can connect to wireless devices through technologies such as Bluetooth, GPRS (general packet-radio service), and GSM (global-system-for-mobile) communications.

Using these technologies, you can develop a wireless-sensor network and control it with LabView. You can also download drivers for numerous proprietary wireless-sensor networks, and, using the LabView Wireless Toolkit, you can test wireless devices that use any of these technologies.

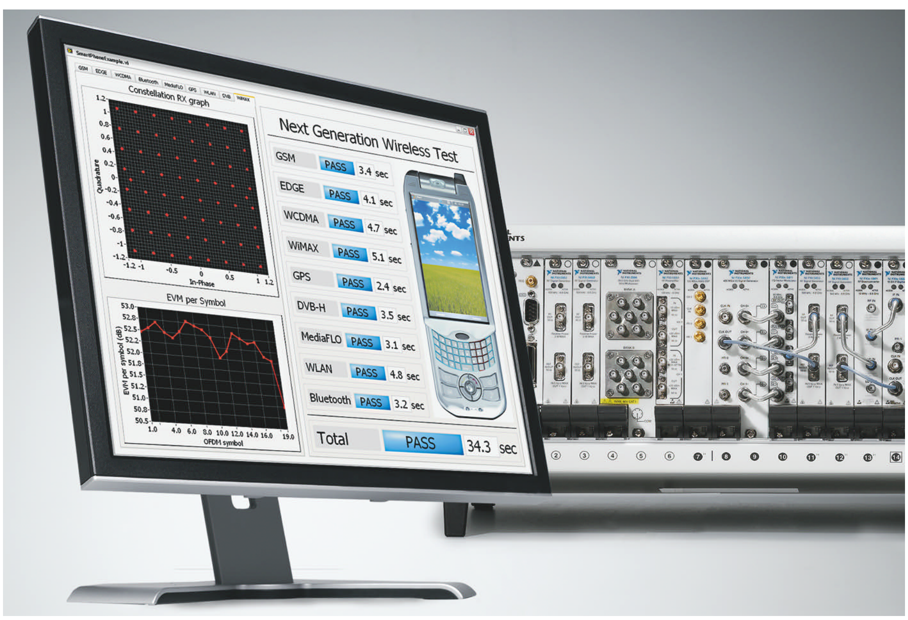
Engineers often use sensors to collect data on mechanical devices, and, with LabView 8.6, you can collect simulations of mechanical devices and then collect data on a real device and integrate the data into the model. This feature lets you see how the model reacts so you can make any necessary design changes.

Multicore processors let computers perform tasks in parallel. LabView 8.6 can automatically assign a processor to a task, or you can optimize your system by assigning processors to tasks. Using multicore processors, you can run automated test functions in parallel and improve system throughput. LabView 8.6 also has more than 1200 data-analysis functions for multicore processors. LabView lets you program custom functions into NI's CompactRIO (reconfigurable-input/output) line of measurement modules, but, with previous versions, you had to directly program a module's FPGA. With LabView 8.6, you no longer need to program the FPGA. Instead, you can use new development and integration features to add functions to an FPGA. Predefined functions include FFTs (fast Fourier transforms) so that you can convert data to the frequency domain in the module.

The software lets you convert LabView applications into Web services that run on desktop or real-time processors. Users can gain access to your applications through any Web-enabled device, including smart phones, PDAs (personal digital assistants), and PCs. This new feature in LabView 8.6 means that you can develop remote user interfaces for your applications using technologies such as HTML (Hypertext Markup Language), JavaScript, and flash. The software has a base price of $1199.

–by Martin Rowe

▷**National Instruments**, www.ni.com/labview86.



LabView 8.6 software provides multicore-optimized analysis and signal-processing functions to increase the performance of automated-test systems, such as wireless-device testers.

DILBERT By Scott Adams

24-bit delta-sigma ADC includes PGA

Analog Devices' AD7190 delta-sigma converter includes the functions to make a complete precision-measurement front end. In addition to the 24-bit converter, the part features a PGA (programmable-gain amplifier) configurable for gains of one to 128. The device also has an internal multiplexer to provide for two differential-measurement sources or four pseudo-differential sources. It incorporates an internal clock source, a temperature sensor, and a bridge-power-down circuit to allow power savings by deactivating the bridge that the part is measuring. The high-precision converter, which can detect an open-sensor condition, suits use in strain gauges, scales, process measurement, control modules, scientific instrumentation and chromatography instruments, and other high-resolution data-acquisition tasks.

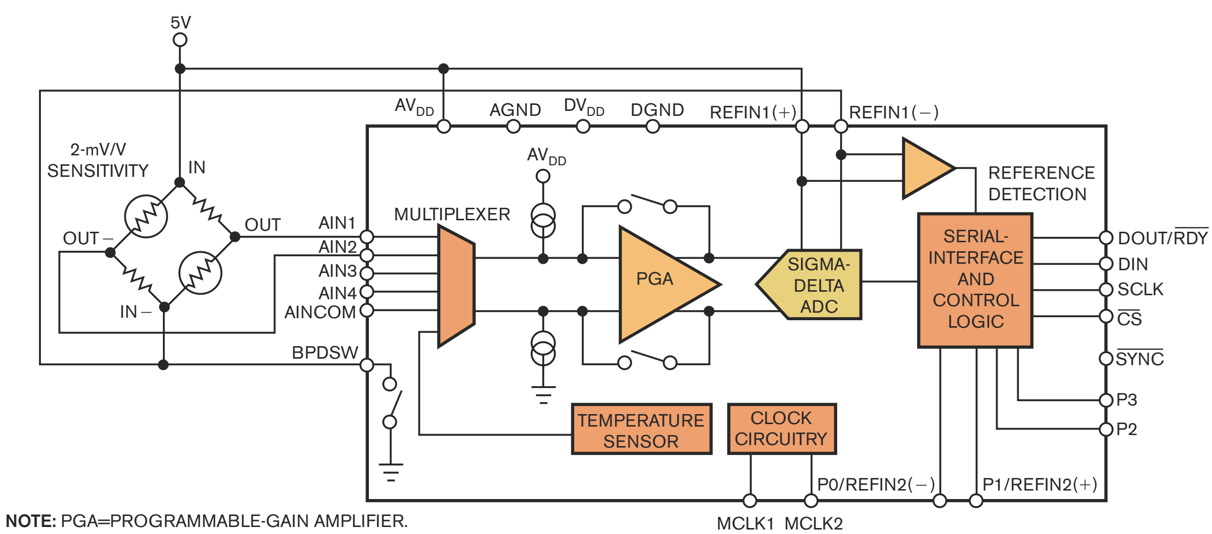
Operating with 3 to 5.25V of power, the AD7190 consumes 6 mA of current; rms noise is 7 nV at a gain of 128. The offset drift is 5 nV/°C, and gain drift is 2 ppm/°C.

The device produces noise-free, 21-bit measurements at 4.7 Hz and 16.5-bit, noise-free measurements at 2.4 kHz, and it performs simultaneous 50- and 60-Hz rejection on an incoming signal. The ADC interfaces to the digital system using an SPI (serial-peripheral interface) or Microwire-compatible interface. You can select a no-latency mode to reduce software overhead if you need a valid conversion per output data. The device also has four general-purpose digital outputs, although two of these outputs also serve as alternative external-reference inputs.

The AD7190 is available in a 24-pin TSSOP for a suggested retail price of $5.90 (1000). It operates over a −40 to +105°C temperature range. Samples are available now, and production quantities will be available in November. An evaluation kit interfaces to a PC with a USB.

—by Paul Rako

▷**Analog Devices**, www.analog.com.



The AD7190 combines a 24-bit ADC with a PGA, a temperature sensor, a bridge power-down, and clock circuits. It is ideal for measuring Wheatstone-bridge outputs.

PICOCHIP OPTIMIZES PROCESSOR-ARRAY CHIPS FOR FEMTOCELLS

PicoChip's second-generation PC3xx family devices integrate the company's modem architecture in a form that will increase performance and reduce the bill-of-materials cost for femtocell manufacturers.

The first of the new family, the single-chip PC302, for HSPA (high-speed-packet-access) femtocells complies with the TR25.820 standard. It supports as many as four residential and small-business users with downlink data rates of 14.4 Mbps and uplink data rates of 5.5 Mbps.

Unlike the fully software-defined approach of PicoChip's PC202 chip, the 302 "hardens" into silicon the features for a WCDMA (wideband-code-division-multiple-access)/HSPA-femtocell design. It employs hardware acceleration of key features of the standard and reduces to approximately 80 the number of processors in the company's signature multiprocessor array.

In 65-nm technology, the 302 integrates a 3GPP (Third Generation Partnership Project) Node B modem, RNC (radio-network controller) stack, RRM (radio-resource management), network-listening functions, and other peripherals. The software-defined architecture of the processor array allows for in-service upgrades and has processing-power margin to host customer-specific functions and other home-networking functions.

The chip is available for sampling now, and volume production will begin in mid-2009.—by Graham Prophet

▶PicoChip, www.picochip.com.

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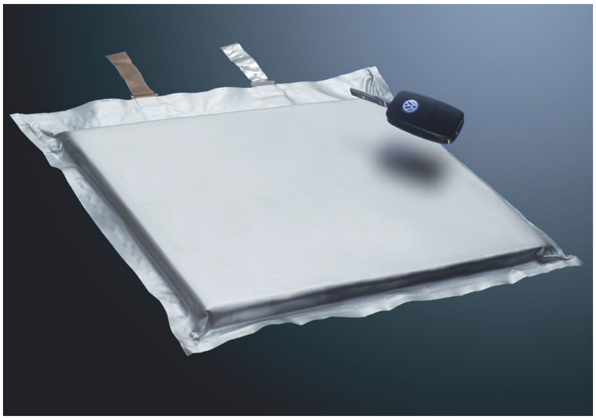


This prototype lithium-polymer accumulator could extend the range and reduce the environmental damage from hybrid vehicles (courtesy Fraunhofer Institute for Silicon Technology).

RESEARCH UPDATE

BY RON WILSON

Lithium-polymer accumulator provides hybrid vehicles with staying power

Now that hybrid passenger cars have scored an enormous marketing success in North America, the struggle has begun to make them competitive with comparable gasoline-powered and diesel vehicles in delivered fuel efficiency and environmental impact. Much of this work focuses on the huge, heavy, short-lived, and environmentally costly battery packs that store energy the vehicles capture from their internal-combustion engines and recapture from their own momentum.

Over the next three years, the Fraunhofer Institutes in Germany will collaborate with Volkswagen to explore lithium-polymer accumulators as alternatives to the lithium-ion batteries today's vehicles often use. The four organizations are working under a development program that Germany's Federal Ministry of the Environment and other organizations launched.

The Fraunhofer portion of the project includes three interrelated programs. In one program, researchers are investigating new electrode materials that will have high energy-storage density but low impact on the environment. A second portion of the project is developing IC-based battery-management techniques that will control such variables as current and temperature to allow much denser packing of cells than is currently feasible. The third program is developing the power electronics to allow the control circuitry to manage safely charging and discharging of the cells. The researchers will integrate all three technologies—the new cells, the new management circuitry, and the new power devices—into a high-density module for use in vehicles.

The goal of the project is for Volkswagen to begin field tests of the new power modules in 2010. The company would presumably later incorporate the modules into a new generation of hybrid vehicles.

▷**Fraunhofer Institute for Silicon Technology**, www.isit.fraunhofer.de.

9.18.08

SELF-ASSEMBLING POLYMERS MAY CREATE TOOLS FOR PATTERNING STORAGE MEDIA

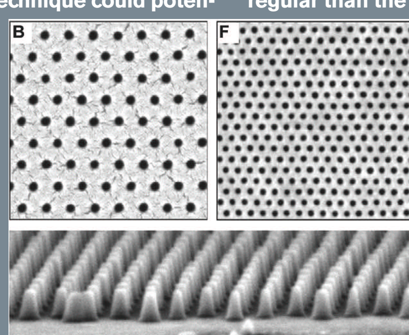
Researchers at the Nanoscale Science and Engineering Center at the University of Wisconsin–Madison, working in collaboration with researchers at Hitachi Global Storage Technologies, have demonstrated the use of self-assembling polymer molecules to create regular molecular-level structures that organize themselves around a relatively coarse chemical pattern. The technique could potentially form mechanical templates that, through nanoimprint lithography, would produce patterned media far denser than researchers can obtain with traditional approaches, boosting the bit density for rotating media beyond the current technical horizon.

The technique relies on the thermodynamic forces within block-copolymer molecules, according to Paul Nealey, the director at the center. The polymer chains contain internal structures that cause them to self-assemble into patterns around a chemical marker. By correctly creating the polymer, researchers caused the molecules to self-assemble into an array of conical towers—just the right shape for use in nanoimprint lithography.

Because the self-assembly process depends on the structure of the molecules rather than upon external direction, the resulting shapes can be more precise and regular than the patterns around which they self-assemble. In this work, for example, the self-assembly process produced an array of towers at one-fourth the pitch of the underlying chemical-marker pattern.

An application would be production of the templates manufacturers use to create patterns on the surface of patterned magnetic media for disk drives. The self-assembling copolymer should be able to produce a regular pattern with more than 10 times the areal density achievable through conventional lithography.

▶**University of Wisconsin, Nanoscale Science and Engineering Center, www.nsec.wisc.edu.**



Researchers prepared a surface with traditional lithography (upper left), upon which a block copolymer material self-assembled into a more detailed pattern (upper right). This approach produced an array of pillars (bottom).

BY HOWARD JOHNSON, PhD

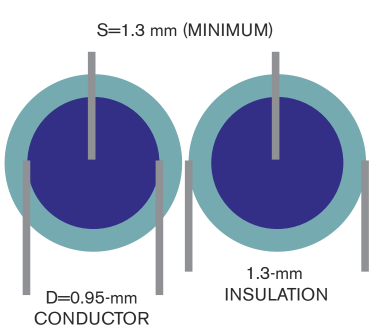
Twisted impedance

Oliver Kent of Muirhead Aerospace Ltd recently commented on my formula for twisted-pair line impedance (**Figure 1**). "I am using coated wire with 1.3-mm outer diameter and 0.95-mm inner diameter," Kent wrote. "The insulation is PTFE [polytetrafluoroethylene] with a dielectric constant, ϵ_R, of 2. Your formula contains the term ln((2S)/D). That term gives a negative value when twice the wire separation over the conductor diameter is less than 1. I appreciate any help or advice you could give regarding this matter."

Kent may be interpreting the spacing as the distance between the wires. I don't. In my system of units, I define the wire spacing from center to center (**Figure 1**). The spacing therefore always exceeds the diameter, so the ratio 2S/D always exceeds 2, and the logarithm cannot go negative.

The simple approximation in **Figure 1** is not perfect. In the real world, if you could press the wires closer and closer together, the impedance would plummet to zero. The approximation doesn't show that result. In the **equation**, when the metallic conductors touch with S equal to D, the term ln((2S)/D) gives a minimum value of ln(2)=0.693, which is incorrect.

I derived the approximation for use only in cases with a reasonably large spacing between wires, in which you may assume a uniform distribution of current around the periphery of each conductor. In a situation with closely spaced wires, the "proximity effect" generates a nonuniform distribution of current, with the greatest preponderance of current occurring on the inside-facing surfaces of the two conductors. Because the approximation does not take into account the proximity effect, it overestimates the impedance in situations with closely spaced wires.



$$Z_{DIFF} \approx \frac{120}{\sqrt{\varepsilon_R}} \ln\left(\frac{2S}{D}\right),$$

WHERE Z IS THE DIFFERENTIAL IMPEDANCE, S IS THE CENTER-TO-CENTER SPACING, D IS THE DIAMETER, S ALWAYS EXCEEDS D, AND 2S/D ALWAYS EXCEEDS D.

EXAMPLE:

$$\frac{2S}{D} = \frac{2(1.3)}{0.95} = 2.736.$$

Figure 1 The differential impedance of this twisted-pair configuration depends on the ratio of spacing, S, to conductor diameter, D.

For ordinary twisted-pair wires in a 100Ω configuration, the ratio S/D is approximately 2. The redistribution of current due to the proximity effect in that case remains fairly modest, producing only a 15% increase in effective resistance and a negligible effect on impedance. In Kent's case, the proximity effect will be more noticeable.

Another difficulty with the approximation involves the concept of "effective dielectric constant." The fields surrounding the wires exist partly in the dielectric insulation and partly in the air surrounding the whole configuration. The effective dielectric constant, therefore, lies between that of air, which is 1, and that of PTFE, which is 2. The exact value takes into account the relative proportions of field energy in those two substances.

Unfortunately, unless you have a 2-D field solver handy, you can't know in advance the relative proportions of field strength in air and insulation, so you can't compute, from first principles, the effective dielectric constant. In that case, you should measure the velocity of propagation on a sample cable and use that measurement to determine the effective dielectric constant. The relation of velocity to dielectric constant is: velocity (m/sec)=speed of light (m/sec)/$\sqrt{\epsilon_{R(EFFECTIVE)}}$.

Once you have obtained a value for the effective dielectric constant, plug that value into the approximation to determine the expected impedance and, more important, the expected change in impedance with changes in geometry. The effective dielectric constant does not vary much with small changes in the wire geometry. **EDN**

Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. Visit his Web site at www.sigcon.com or e-mail him at howie03@sigcon.com.

+ **www.edn.com/signalintegrity**

BY JOSHUA ISRAELSOHN, CONTRIBUTING TECHNICAL EDITOR

Know your ceramic capacitor, part one

Although advancements in dielectric materials and fabrication processes have improved integrated capacitors, chip designers still depend on board-level devices to support virtually all ICs. Primary tasks for board-level capacitors are power-supply bypassing and signal coupling, but many ICs still depend on external parts for timebase generation, filtering, and waveform shaping.

Driven largely by matters of size, cost, and availability, multilayer ceramic is among the most common capacitor constructions in the industry. This trend has accelerated over the last several years, during which tantalum prices more than quadrupled, making volumetrically efficient tantalum capacitors more expensive and less available than they historically have been.

The EIA (Electronic Industries Alliance) associates ceramic capacitors with four classes, of which the first three are in widespread use today (**Reference 1**). Three-character alphanumeric designations within a class characterize the capacitor's thermal behavior. The significance of the designators, however, is class-specific.

Class I ceramic capacitors are temperature-compensated and, therefore, provide the most stable performance of all the classes. The EIA designators for Class I capacitors describe the device's temperature coefficient of capacitance. The designator's three characters provide a mantissa, a multiplier, and a tolerance (**Table 1**, available in the Web version of this column at www.edn.com/080918ji).

The most common Class I capacitor carries the designation C0G, and nominally provides a zero temperature coefficient of capacitance with a ±30 ppm/°C tolerance over a 25 to 85°C range. Note that the temperature range over which the temperature coefficient of capacitance and its tolerance apply is not the capacitor's full operating-temperature range. To the extent that C0Gs deviate from their ideal zero temperature coefficient of capacitance, their drift tends to be linear with temperature. Some manufacturers, therefore, specify their C0G capacitors' drift within the ±30 ppm/°C band from −55 to +125°C.

> **Class I capacitors exhibit a low-voltage coefficient of capacitance, an important attribute in signal-processing circuits in which low distortion is a requirement.**

Class I capacitors also exhibit a low-voltage coefficient of capacitance, which is an important attribute in signal-processing circuits in which low distortion is a requirement. This observation isn't to suggest that a Class I capacitor—or any ceramic capacitor, for that matter—is your best choice for critical signal-processing circuits. However, if your application doesn't require the precision of, say, instrumentation-quality measurement circuits or professional-quality audio equipment, you'll be hard-pressed to find a more compact, inexpensive, and readily available capacitor than a multilayer ceramic.

For high-frequency applications, Class I ceramic capacitors exhibit lower parasitic series inductances and thus higher resonant frequencies than do devices of Class II and higher. RF-rated C0G capacitors with values as large as 50 pF typically exhibit resonant frequencies in excess of 1 GHz.

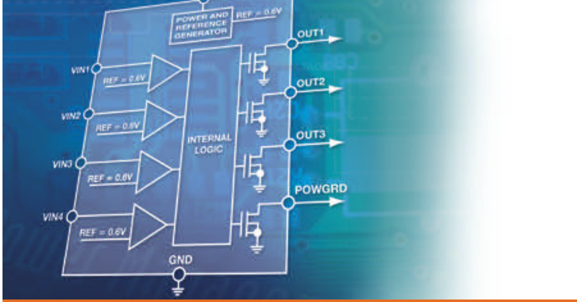
Class I multilayer ceramic capacitors are readily available in surface-mount form factors in capacitances as large as 10 nF. Some suppliers provide surface-mount devices with capacitances as large as 100 nF and leaded devices in excess of 1 μF. Owing to their limited dielectric constants, typically in the range of 10 to 100, Class I devices at the upper end of the technology's capacitance range tend to be quite large. The higher dielectric constant of Class II ceramics produces more compact devices with a wider range of capacitances than do Class I ceramics—the next subject in *Analog Domain*. EDN

REFERENCE

1 "Ceramic dielectric capacitors classes I, II, III, and IV," Electronic Industries Alliance, Standard EIA 198-1F.

Joshua Israelsohn is a co-founder of JAS Technical Media, where he manages technical-communication services. You can find his contact information at www.jas-technicalmedia.com/Contact.

+ www.edn.com/analogdomain



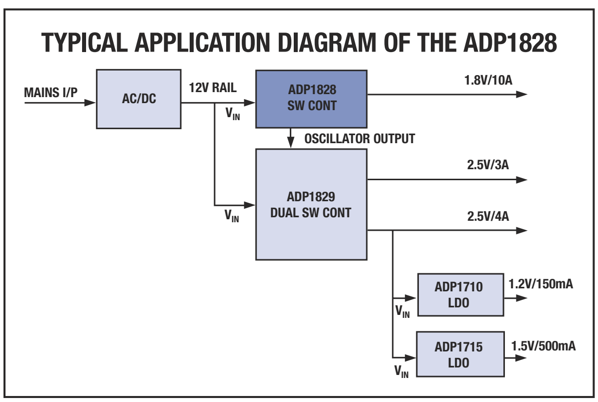
POWER AND THERMAL MANAGEMENT ICs

YOUR SEMICONDUCTOR SOLUTIONS RESOURCE
Volume 8, Issue 6

Contents

On-Board Oscillators Synchronize Other Regulators to Reduce the Number of Beat Frequencies

Many systems are highly sensitive to noise and beat frequencies. When using switching regulators, this challenge is typically amplified by the fact that each regulator is running at a different frequency, thus generating a number of beat frequencies that are difficult to filter out. One approach to overcome this challenge is to run all switching regulators at the same switching frequency. However, to achieve this solution, all regulators need to be synchronized to the same oscillator. Rather than requiring placement of an oscillator circuit on a board, the oscillator output of ADI's ADP1828 dc-to-dc controller can be used to synchronize other controllers. The switching frequency is user programmable from 300 kHz to 600 kHz with a single resistor. The synchronization output frequency can be phase shifted 180° to reduce the size of input capacitors or it can be doubled with a pin setting to provide the 2× frequency that some switches require.



The ADP1828 generates a switching frequency that can be used to synchronize other regulators.

ADP1828 Features

- Wide supply range: 3 V to 18 V
- Oscillator frequency output to allow synchronization to other controllers
- Accuracy over temperature: ±0.85%
- Efficiency: up to 95%
- Shutdown current: 15 μA

Part Number	V_{IN} Range (V)	V_{OUT} Adj Options (V)	I_{OUT} Max (A)	Switch Freq	Package	Price ($U.S.)
ADP1821[1]	3.7 to 5.5	0.6 to 0.85 V_{IN}	20	600 kHz[2]	16-lead QSOP	1.35
ADP1822[1]	3.7 to 5.5	0.6 to 0.85 V_{IN}	20	600 kHz[2]	24-lead QSOP	1.40
ADP1828[1]	3 to 18	0.6 to 0.85 V_{IN}	20	600 kHz[2]	20-lead QSOP	1.50
ADP1829[1]	3 to 18	0.6 to 17	20	600 kHz[2]	32-lead LFCSP	2.10
ADP1864[1]	3.15 to 14	0.8 to V_{IN}	5	580 kHz	6-lead TSOT	1.05
ADP2102[3]	2.7 to 5.5	0.8 to 1.2, 1.2 to 1.5, 1.5 to 1.8, 2.5 to 3.3	0.6	3 MHz	8-lead LFCSP	1.47
ADP2105[3]	2.7 to 5.5	0.8 to V_{IN}	1	1.2 MHz	16-lead LFCSP	1.13
ADP2106[3]	2.7 to 5.5	0.8 to V_{IN}	1.5	1.2 MHz	16-lead LFCSP	1.25
ADP2107[3]	2.7 to 5.5	0.8 to V_{IN}	2	1.2 MHz	16-lead LFCSP	1.32
ADP3050[3]	3.6 to 30	—	1.5	200 kHz	8-lead SOIC	1.78

[1]Step-down type. [2]From 300 kHz to 600 kHz, synchronization up to 1 MHz. [3]Buck type.

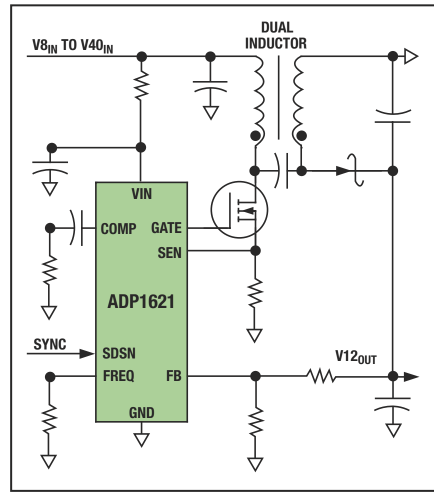
DC-to-DC Controller Provides Steady Voltage No Matter What the Input

The ADP1621 is a fixed frequency, pulse-width modulation, current-mode, step-up controller. It is ideal for a SEPIC (single-ended primary inductor converter) configuration because it enables the output voltage to be above, below, or equal to the input voltage, as necessary. This configuration is useful in an application where battery voltage can be above or below the output voltage that it is trying to control.

A SEPIC is just one of many configurations that the ADP1621 can help optimize. For example, it can also be used in forward and flyback configurations, as well as in a boost mode configuration, where it can boost the voltage from below 5 V to over 50 V, as needed.

ADP1621 Features

- Accuracy: ±1%
- Lossless current sensing for switch-mode voltage: ≤30 V
- Resistor current sensing for switch-mode voltage: ≥30 V
- Current-mode operation for excellent line and load transient response
- Current-limit and thermal overload protection
- Package: 10-lead MSOP



SEPIC configuration allows V_{OUT} to be greater or less than V_{IN}.

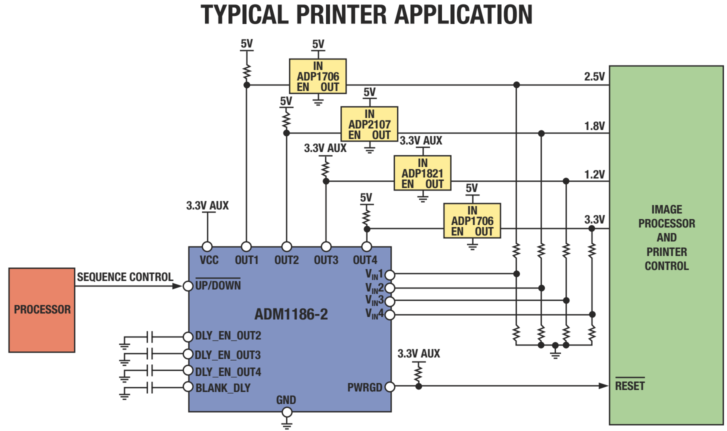
Part Number	Type	V_{IN} Range (V)	V_{OUT} Preset Options (V)	V_{OUT} Adj Options (V)	I_{OUT} Max (A)	Switching Frequency	Package	Price ($U.S.)
ADP1111	Boost	2 to 30	3.3, 5, 12	—	1.5	70 kHz	8-lead plastic DIP, 8-lead SOIC	2.06
ADP1610	Boost	2.5 to 5.5	—	V_{IN} to 12	1.2	700 kHz or 1.2 MHz	8-lead MSOP	1.25
ADP1621	Multi	8 to 40	—	—	—	300 kHz or 1.2 MHz	10-lead MSOP	1.30

Industry's Highest Accuracy (±0.8%) Voltage Sequencers and Supervisors

Today's complex systems often require up to four voltages and more accurate monitoring, as well as power-up and power-down supply sequencing of the voltage rails. There is a growing trend toward lower core voltages, driven by newer, smaller process geometries. These low voltages need to be monitored accurately and then powered up and powered down in the correct sequence while ensuring the correct timing delay between each of the voltage rails. If the power supply voltage drops below the threshold or is powered up or powered down incorrectly in a printer ASIC, for example, the device can operate erratically, potentially causing a loss of data.

The ADM1186 family provides ±0.8% voltage threshold monitoring accuracy, which is critical when monitoring low voltage rails. This monitoring is illustrated in the printer application example, shown below. The ADM1186 also provides power-up and power-down supply sequencing implemented using a digital core. In the case of the ADM1186-1, multiple devices can be cascaded to sequence up and sequence down eight, 12, 16, or more supplies. Dedicated capacitor programmable timing pins allow the time delays between supplies to be more easily and accurately controlled without requiring a capacitor on the supply rail monitoring pin. This flexibility allows the sequencing time delay and the fault response time of the device to be controlled independently and accurately. In addition to the sequence time delays, a programmable blanking time delay is provided to allow the designer to set a maximum time limit for a supply to rise above its undervoltage threshold after being enabled.

VOLTAGE MONITORING AND SEQUENCING IN A TYPICAL PRINTER APPLICATION



(See the voltage sequencers and supervisors selection tables on Page 3 for product details.)

Voltage Sequencers and Supervisors Selection Tables

Quad Voltage Sequencers

Part Number	Number of Monitored Voltages	Voltage Monitoring Accuracy (±%)	Number of Output Drivers	Sequencing		Active High Enable Output	Sequence Delay	Package	Price ($U.S.)
				Up	Down				
ADM1184	4 (cascadable)	0.8	4	Yes	No	Open-drain	—	10-lead MSOP	2.39
ADM1185	4 (cascadable)	0.8	4	Yes	No	Open-drain	190 ms	10-lead MSOP	1.20
ADM1186-1	4 (cascadable)	0.8	4	Yes	Yes	Open-drain	Capacitor (adj)	20-lead QSOP	3.80
ADM1186-2	4	0.8	4	Yes	Yes	Open-drain	Capacitor (adj)	16-lead QSOP	2.98

Multivoltage Supervisors

Part Number	Number of Monitored Voltages	Reset Threshold (V)	Min Reset Timeout (ms)	Reset Output Stage		Manual Reset Capability	Typ Watchdog Timeout (ms)	Package	Price ($U.S.)
				Active Low	Active High				
ADM13305	2	0.6 (adj), 1.25 (adj), 1.68, 2.25, 2.93, 4.55	140	Push-pull	Push-pull	Yes	1600	8-lead NSOIC	0.95
ADM13307	3	0.62 (adj), 1.58, 1.67, 2.19, 2.32, 2.93, 3.08, 4.38, 4.63	140	Push-pull	Push-pull	Yes	—	8-lead NSOIC	0.98
ADM6710	3 or 4	0.6 (adj), 1.58, 1.67, 2.19, 2.32, 2.63, 2.78, 2.93, 3.08, 4.38, 4.63	140	Open-drain	—	No	—	6-lead SOT-23	1.60
ADM1184	4	0.6 (adj)	100	Open-drain	—	No	—	10-lead MSOP	2.39

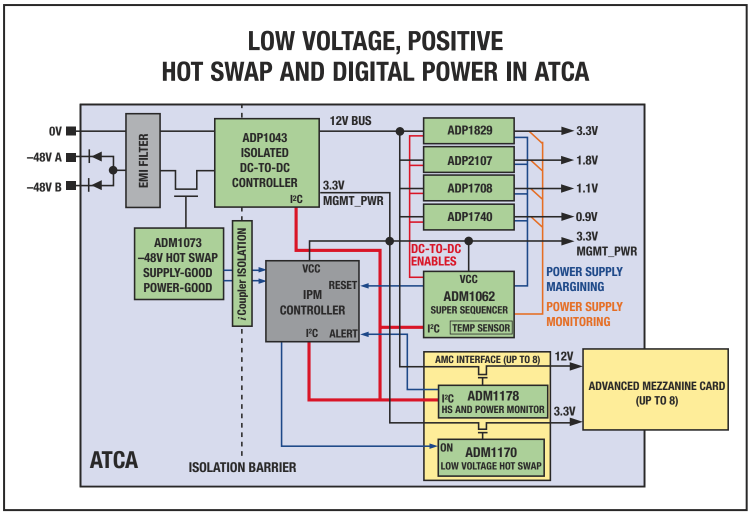
Precision Voltage References for Lower Current Applications

Analog Devices offers several families of precision references targeting applications requiring low drift, low noise, and small size. Output currents up to 30 mA are available with a temperature coefficient as low as 2 ppm/°C. Several devices are available in 3-lead SC70 and SOT-23 packages that are ideal for space-critical applications.

Part Family	V_{OUT} (V)	Initial Accuracy (±%)	Tempco (ppm/°C)	Output Noise (μV p-p) @ 2.5 V_{OUT}	Output Current (mA)	Package	Price ($U.S.)
ADR0x	2.5, 3, 5, 10	0.06	3	6	10	5-lead SC70, 5-lead TSOT, 8-lead SOIC	1.02
ADR43x	2.048, 2.5, 3.0, 4.096, 4.5, 5	0.04	3, 10	3.5	10	8-lead MSOP, 8-lead SOIC	2.92
AD158x	2.5, 3, 4.096, 5	0.08	50	70	5	3-lead SOT-23	0.60
ADR504x	2.048, 2.5, 3, 4.096, 5	0.1	75	9	N/A (shunt reference)	3-lead SC70, 3-lead SOT-23	0.30
REF19x	2.048, 2.5, 3, 3.3, 4.5, 5	0.2	2	25	30	8-lead TSSOP, 8-lead SOIC	1.25

ADI Introduces the World's Most Accurate Hot Swap Controllers with Integrated Digital Power Monitors

The advanced telecom computing architecture (ATCA) and microtelecom computing architecture (MicroTCA) modular systems share a common pluggable form factor—the advanced mezzanine card (AMC). When an AMC is plugged into an ATCA card or MicroTCA shelf host, it requests that the host processor allocate a portion of the available system power budget for the AMC itself. After allocating power to the AMC, the host must then monitor each AMC so that it does not consume more than its allowed power budget. An AMC drawing too much power may indicate a fault on the card. If the draw becomes excessive, it could exceed the total available system power, adversely affecting the operation of the host. Therefore, it is important in applications such as these that the host is able to accurately monitor the power consumption of each AMC individually.



To meet these requirements, ADI's family of hot swap and power monitors provides a new standard of performance and value for computing and telecom systems. For example, the ADM1178 integrates a low voltage positive hot swap controller with a current-sense amplifier to provide digital current and voltage monitoring. This functionality is enabled by an on-chip, 12-bit ADC that communicates through an I²C® interface. The process allows a card to be hot swapped safely in the application, while also providing power consumption information from the card to the host controller via the I²C bus. The device provides a single-chip, integrated hot swap and power monitoring solution with the smallest footprint in the industry.

Low Voltage Hot Swap and Power Monitors

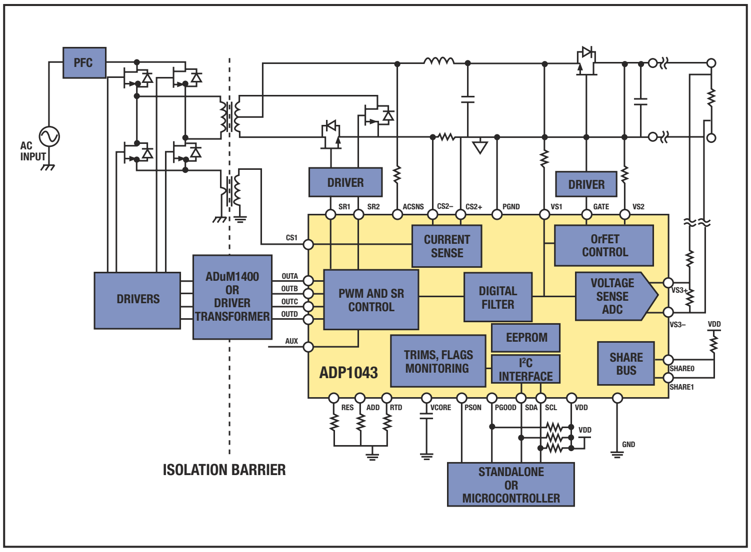
Part Number	Operating Range (V)	UV and OV Detection	Digital V and I Readback	Current Monitoring Accuracy (±%)	Other Inputs	Other Outputs	Package	Price ($U.S.)
ADM1170	1.6 to 16.5	ON (UV)	—	—	—	—	8-lead TSOT	2.10
ADM1171	2.7 to 16.5	ON (UV)	—	—	—	CS_OUT	8-lead TSOT	2.20
ADM1172	2.7 to 16.5	ON (UV)	—	—	PFI	PFO	8-lead TSOT	2.00
ADM1175	3.15 to 16.5	ON (UV), ONB (OV)	I²C Interface with 4 addresses	2	CONV	—	10-lead MSOP	2.50
ADM1176	3.15 to 16.5	ON (UV)	I²C Interface with 16 addresses	2	—	—	10-lead MSOP	2.50
ADM1177	3.15 to 16.5	ON (UV)	I²C Interface with 4 addresses	2	—	—	10-lead MSOP	2.50
ADM1178	3.15 to 16.5	ON (UV)	I²C Interface with 4 addresses	2	—	ALERTB	10-lead MSOP	2.70
ADM4210	2.7 to 16.5	ON (UV)	—	—	—	—	6-lead TSOT	2.98

Power Monitors

Part Number	Operating Range (V)	Current Monitoring Accuracy (±%)	Glitch Filter	CONV Pin	CLRB Pin	ALERT/ ALERTB	Digital V and I Readback	Package	Price ($U.S.)
ADM1191	3.15 to 26	2	—	Yes	No	ALERTB	I²C interface with 4 addresses	10-lead MSOP	1.90
ADM1192	3.15 to 26	2	Programmable timer	No	Yes	ALERT	I²C interface with 16 addresses	10-lead MSOP	1.90

New Digital Controller Dramatically Increases System Efficiency and Accelerates Time to Market

Demand for increased energy efficiency has become a common industry expectation in server, storage, and communications infrastructure applications. The ADP1043 is a digital controller designed for ac-to-dc and isolated dc-to-dc intermediate bus architectures that enable high efficiency designs in end-user equipment. The device has seven programmable PWM outputs to drive even the most complex and high efficiency conversion architectures. The programmability of the ADP1043 allows the system designer to better configure circuit parameters, such as timing delays, to optimize efficiency. The flexibility provided allows the system designer to make dynamic changes to improve efficiency across the application load range.



All programming is performed with an easy to use graphical user interface (GUI)—where no complex programming is required. The ADP1043 and GUI solution promote faster design time to market.

ADP1043 Features

- Digital control and monitoring
- Outputs: 7 PWM
- Programmable switching frequency: 50 kHz to 700 kHz
- Programmable digital filter/compensator
- Active OR'ing control
- Analog or digital current sharing
- I²C communication and programming
- On-board EEPROM
- Reporting and diagnostic capabilities

Temperature Control Independent of the Microprocessor

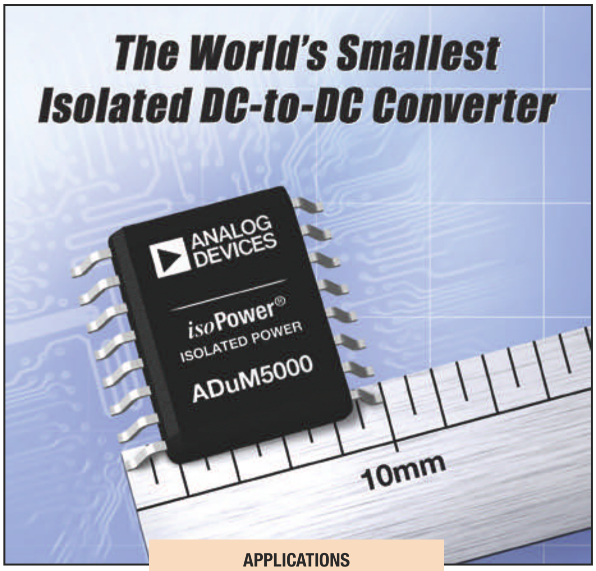
The ADT6401 and ADT6402 are pin-selectable temperature trip points available in 6-lead SOT-23 packages. Each part contains an internal band gap temperature sensor for local temperature sensing. When the temperature crosses the trip point setting, the logic output is activated. These ICs are excellent fail-safe devices with the capability of monitoring temperature independent of the microprocessor. The ADT6401 logic output is active low and open-drain. The ADT6402 logic output is active high and push-pull. The pin-selectable trip point settings are 10°C apart, starting from –45°C to +5°C for undertemperature switching and from –45°C to +115°C for overtemperature switching. These devices typically consume only 30 µA of supply current and operate over the supply range of 2.7 V to 5.5 V. Hysteresis is pin-selectable at 2°C and 10°C.

Part Number	Trip Point Type	Trip Threshold	Trip Output	Supply Current Max (µA)	Comments	Package	Price ($U.S.)
ADT6401	Pin-selectable	Hot, cold	Active low, open-drain	50	Connect pins 1, 3, 5 either high, low, or floating to determine trip point	6-lead SOT-23	0.59
ADT6402	Pin-selectable	Hot, cold	Active high, push-pull	50	Connect pins 1, 3, 5 either high, low, or floating to determine trip point	6-lead SOT-23	0.59
ADT6501	Factory set	Hot	Active low, open-drain	85	Preprogrammed trip point	5-lead SOT-23	0.49
ADT6502	Factory set	Hot	Active high, push-pull	85	Preprogrammed trip point	5-lead SOT-23	0.49
ADT6503	Factory set	Cold	Active low, open-drain	85	Preprogrammed trip point	5-lead SOT-23	0.49
ADT6504	Factory set	Cold	Active high, push-pull	85	Preprogrammed trip point	5-lead SOT-23	0.49

All parts operate from 2.7 V to 5 V with trip point temperature increments of 10°C from –45°C to +115°C. Operates fully from –55°C to +125°C.

Reduce Space Requirements Needed for Isolated DC-to-DC Power Supply

The ADuM5000 is the world's smallest isolated dc-to-dc converter. Available in a compact 10 mm × 10 mm, 16-lead wide-body SOIC package, it is a full 40% smaller than the closest competitor's dc-to-dc converter solution. The ADuM5000 provides up to 500 mW of regulated, isolated power of 3.3 V or 5.0 V. Other *iso*Power® products, such as the ADuM540x and ADuM520x product families, also provide both isolated power and signal channels within a single package. The *iso*Power family of parts offers the designer significant advantages over discrete solutions, such as optocouplers that require an external dc-to-dc converter, and often cuts costs by as much as 50%. The ADuM5000 can be used in combination with ADuM540x and ADuM520x *iso*Power products to achieve higher output power efficiency levels.



APPLICATIONS
- RS-232, RS-422, RS-485 transceivers
- Industrial field bus isolation
- Power-supply start-up bias and gate drive
- Isolated sensor interface
- Industrial PLC

ADuM5000 Features

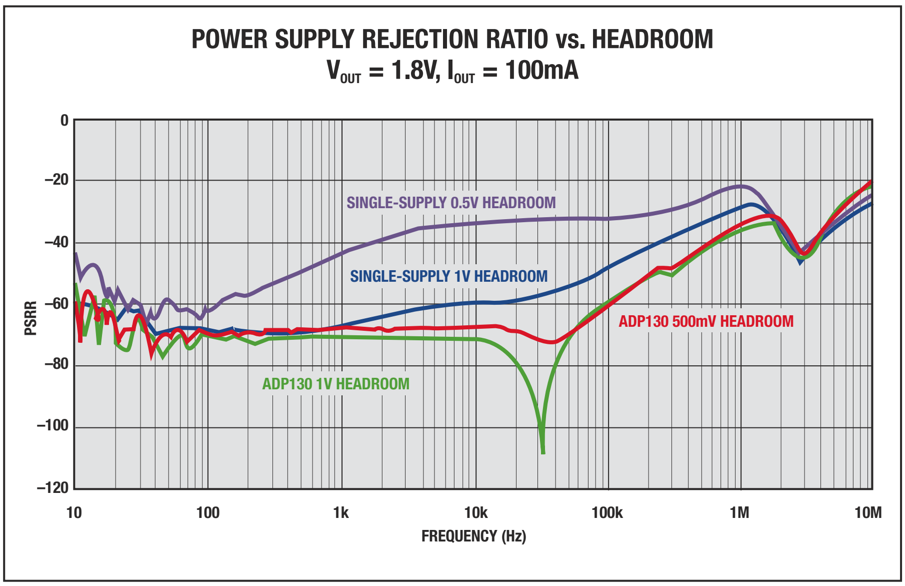
- *iso*Power integrated isolated dc-to-dc converter
- Isolation: 2.5 kV
- Regulated 3.3 V or 5 V output
- Output power: 500 mW for 5 V
- High temperature operation: up to 105°C
- High common-mode transient immunity: >25 kV/µs
- Thermal overload protection
- Safety and regulatory approvals (pending): UL, CSA, VDE
- Package: 16-lead SOIC_W with >8 mm creepage

Part Number	Channel Configuration	UL Insulation Rating (kV)	Max Data Rate @ 5 V (Mbps)	Isolated Output Supply Voltage (V)	Max Isolated Output Supply Current (mA)	Max Operating Temp (°C)	Package	Price ($U.S.)
ADuM5401	3/1	2.5	1 or 25	3.3 or 5	100	105	16-lead SOIC_W	5.00
ADuM5402	2/2	2.5	1 or 25	3.3 or 5	100	105	16-lead SOIC_W	5.00
ADuM5403	1/3	2.5	1 or 25	3.3 or 5	100	105	16-lead SOIC_W	5.00
ADuM5404	0/4	2.5	1 or 25	3.3 or 5	100	105	16-lead SOIC_W	5.00
ADuM5200	2/0	2.5	1 or 25	3.3 or 5	100	105	16-lead SOIC_W	4.08
ADuM5201	1/1	2.5	1 or 25	3.3 or 5	100	105	16-lead SOIC_W	4.08
ADuM5202	0/2	2.5	1 or 25	3.3 or 5	100	105	16-lead SOIC_W	4.08
ADuM5000	—	2.5	—	3.3 or 5	100	105	16-lead SOIC_W	3.16

Improve Conversion Efficiency and Optimize Performance for Low Output Voltages in Post-Regulation Applications

Today's user demands new features and functions, as well as longer battery life, for their mobile electronic devices. System and power management designers are meeting these challenges by using very low dropout regulators (LDOs) to power ICs operating at lower supply voltages.

In low headroom post-regulation applications optimized for high power supply rejection, LDOs with a dual-supply architecture—such as ADI's ADP130—offer an excellent balance of low noise, high power supply ripple rejection, and low quiescent current. Such features make the ADP130 an ideal solution for a clean power supply. The device can be biased from the higher input supply, while the lower input supply sources the load current to reduce the overall power dissipation and allow for low dropout operation. The ADP130 complements ADI's family of clean power, high performance LDO solutions with its unique low dropout option.



The plot above compares the dual-rail ADP130 PSRR of 60 dB up to 100 kHz in low headroom applications vs. a single-supply LDO, which has 20 dB to 30 dB lower PSRR under the same conditions.

ADP130 Features

- Load current: 350 mA
- Dropout voltage: 40 mV @ 150 mA
- Quiescent current: 25 µA @ no load
- PSRR: –70 dB @ 10 kHz
- Noise: 40 µV rms @ 1.5 V

Part Number	I_{OUT} (mA)	V_{IN} Range (V)	V_{BIAS} (V)	V_{OUT} Options (V)	Price ($U.S.)
ADP120	50	2.3 to 5.5	—	1.2 to 3.3	0.26
ADP121	100	2.3 to 5.5	—	1.2 to 3.3	0.26
ADP130	350	1.2 to 3.6	2.3 to 5.5	1.2 to 3.3	0.33

For a complete listing of ADI's LDO product portfolio, visit *www.analog.com/LDO*.

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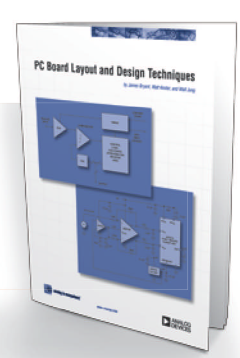

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SiGe PROCESSES CAN GIVE ANALOG-CIRCUIT DESIGNERS FAST, HIGH-VOLTAGE TRANSISTORS WITH LOW NOISE, WHEREAS BiCMOS SiGe FITS INTO CMOS PROCESS FLOWS.

BY PAUL RAKO • TECHNICAL EDITOR

SILICON GERMANIUM: *FAST*, QUIET, and POWERFUL

CMOS (complementary-metal-oxide-semiconductor) processes have consistently surprised the semiconductor industry. CMOS prices decreased and CMOS speeds increased, a scenario that primarily benefits digital-IC designers. A digital-IC designer does not care that a part is running on 1V or less, as long as there is enough SNR (signal-to-noise ratio) to discriminate a one from a zero. Analog-circuit designers, on the other hand, have a much harder time making the myriad trade-offs necessary for a pure-analog-signal or a mixed-signal part. One of the fundamental problems with fine-line CMOS is the high cost of its mask set. That drawback makes the technology available only to large-market ICs that can amortize the cost. Analog-IC designers have alternatives, however: Bipolar SiGe (silicon germanium) and BiCMOS (bipolar-CMOS) SiGe. In addition, germanium-strained-silicon CMOS creates fast PMOS (positive-channel-MOS) transistors that allow for fast, complementary low-leakage digital design.

In germanium-strained silicon, manufacturers implant germanium into the channel of the PFETs (positive-channel field-effect transistors). The presence of the larger germanium atom stretches the silicon lattice, providing faster carrier mobility (**Figure 1**). This process is thus inherently more complementary, with similar-sized transistors for both the negative- and the positive-channel devices. In the hands of a good IC designer, the performance of fast PNP (positive/negative/positive) transistors, even in digital designs that ignore the transistor-level-circuitry benefit, can improve because the technology reduces both die area and cost. Although electronics professors still teach students that the drive currents of NFETs (negative-channel FETs) are three times those of PFETs, some industry observers dispute that idea. "That [assumption] is no

AT A GLANCE

- SiGe (silicon germanium) can be a purely bipolar process, a BiCMOS (bipolar-complementary-metal-oxide-semiconductor) process, or a strained-silicon process in CMOS PFETs (positive-channel field-effect transistors).
- In strained-CMOS PFETs, the germanium increases the mobility of carriers in the P channel.
- In bipolar or BiCMOS processes, the germanium resides in an epitaxial film to create the base region.
- Bipolar SiGe changes the bandgap in the base area and allows higher dopant concentrations.
- SiGe processes use normal fab flows, requiring only the addition of the epitaxial reactor.
- SiGe ICs can use available tool flows.
- SiGe has a niche in analog and RF parts that benefit from the low cost and integration of silicon but do not need the performance of III-V-semiconductors–those combining an element from the third column of the periodic table with an element from the fifth column.

longer true for modern processes," says Ric Borges, senior marketing manager for TCAD (technology-computer-aided design) at Synopsys. "There are even cases where the drive current of the PMOS device is higher than that of the NMOS [negative-channel-MOS] device, due to the strained silicon."

When op-amp or RF designers discuss SiGe, they are generally referring to bipolar SiGe (**Figure 2**). Because bipolar SiGe is not a CMOS process, the bipolar transistors can provide high performance. "SiGe HBTs [heterojunction-bipolar transistors] have SiGe alloys of nanoscale thickness—say, 20% SiGe over 50 nm—embedded in their base regions, which are compositionally graded to boost their performance metrics in a tunable way," says John D Cressler, the Ken Byers Professor at the Georgia Institute of Technology. This alloy results in higher gain, higher frequency, higher maximum frequency, lower-resolution bandwidth, lower noise floor, lower flicker noise, and higher output resistance than a similarly doped silicon-only bipolar transistor, he says. The presence of fast, complementary PNP transistors allows this process to make operational amplifiers with gain-bandwidth products greater than 1 GHz. Just as important, SiGe's lower noise figure helps the amplifier deliver remarkable performance, and its operating voltage can be higher than that of CMOS processes, increasing SNR in RF receivers. This higher voltage is an essential feature of RF-power amplifiers. SiGe also provides better linearity, which is essential in modern modulation schemes in which the RF envelope contains the information (**Reference 1**).

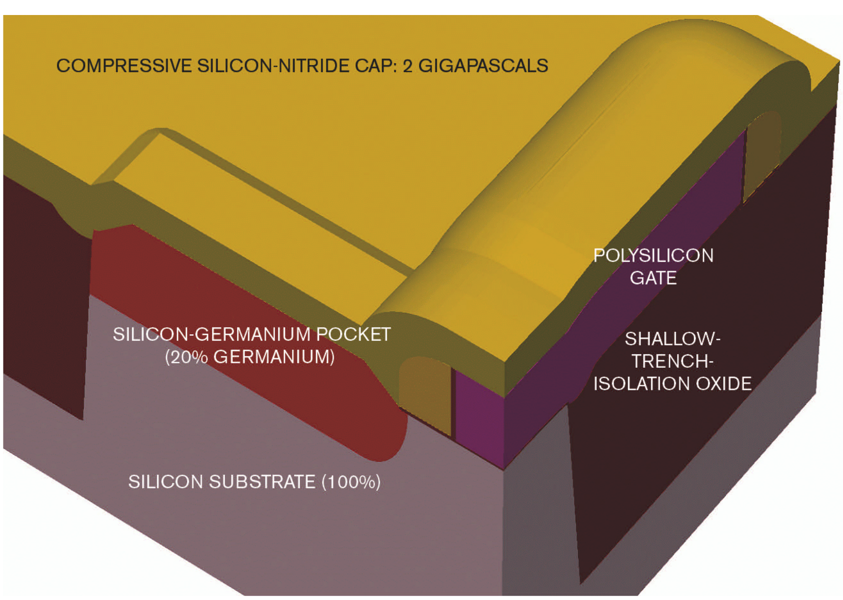


Figure 1 A strained-silicon PFET has germanium in the channel region to increase carrier mobility and, thus, speed (courtesy Synopsys).

"Even in the industrial [market], where you want higher-voltage parts, SiGe is an enabling technology due to the increased beta [current-gain] and early-voltage benefits," says Tim Kalthoff, a TI fellow and chief technologist for high-performance analog at Texas Instruments. "You get higher gain and better precision with better distortion characteristics because of SiGe," he says. SiGe transistors are superior to other bipolar transistors in almost every figure of merit. SiGe exhibits many of the same trade-offs as silicon transistors, but, because its performance metrics are all on a higher baseline, you can tune a SiGe process to surpass the performance of silicon transistors in almost any specification without letting any other specification fall below best in class for silicon. In addition, the process can use not only trench isolation, but also full dielectric isolation for low stray capacitance and maximum speed (**Figure 3**).

These processes are ideal for mixed-signal parts that need the blazing speed of SiGe and the signal-processing control of CMOS. Because the CMOS in these processes is generally two generations old, the line widths are 135 nm or more. This width can provide benefits such as higher-voltage operation, but it also provides a significant cost penalty for the digital part of the chip. For this reason, designers of low-cost, high-volume digital circuits prefer to stick with CMOS if possible and move the RF or analog to a separate chip if they cannot design it in CMOS.

HISTORY OF A PROCESS

In the 1950s, Herbert Kroemer, a professor of physics at the University of California—Santa Barbara, proposed the HBT. Russian physicist Zhores I Alferov, who in 2002 shared the Nobel Prize with Kroemer, independently invented the heterotransistor. Kroemer's research focused on III-V compounds, such as GaAs (gallium arsenide), which are semiconductors that combine an element from the third column of the periodic table and an element from the

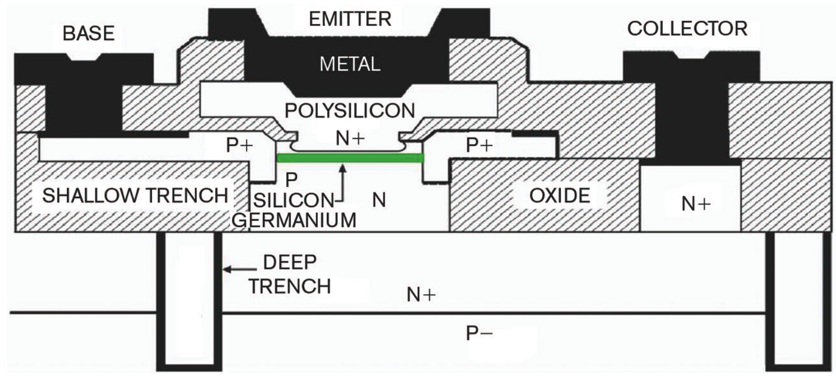


Figure 2 This silicon-germanium NPN HBT has trench-isolated devices on a junction-isolated substrate (courtesy John Cressler, Georgia Institute of Technology).

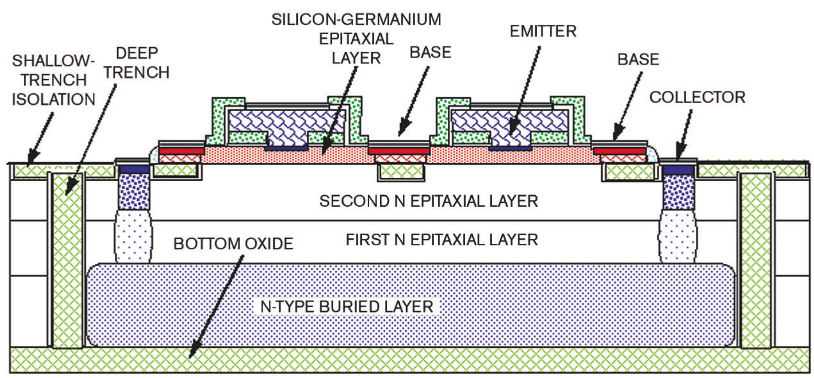


Figure 3 In addition to trench isolation between devices, SiGe processes can use a bottom oxide to achieve full dielectric isolation (courtesy Texas Instruments).

fifth column. By 1987, seeking a process to use in mainframe computers, IBM adapted the HBT to silicon processes (**Reference 2**).

Engineers at the company knew that they could achieve higher speeds with SiGe, but CMOS designs offered lower power consumption—critical to that era's mainframe computers. Knowing that SiGe produced superior transistors, IBM repurposed the SiGe process for use in analog- and mixed-signal RF ICs, using a high-vacuum-deposition system, according to Jeff Babcock, principal integration-device engineer at National Semiconductor (**Figure 4**). Universities, including the Georgia Institute of Technology, are assisting in the development of SiGe processes. Georgia Tech's Professor Cressler has dedicated an entire lab to pursuing this transistor technology to its limits.

Soon, other semiconductor companies started to see the potential for SiGe in their analog designs. Analog Devices in 1993 formed an alliance with IBM, and Texas Instruments developed several similar processes for op amps and RF designs. National Semiconductor also uses multiple SiGe processes, including bipolar SiGe, which finds use in amplifiers, and BiCMOS SiGe, which finds use in interface and mixed-signal products. Maxim Integrated Products is using SiGe to assist in its expansion into RF ICs. Several fabs, including Jazz, NEC, and austriamicrosystems, also offer SiGe processes (**Reference 3**). IBM has not rested on its laurels, either, having recently announced SiGe transistors that have unity-gain frequencies approaching 300 GHz at low temperatures. Researchers expect by the end of the decade to have 500-GHz SiGe as well as 300-GHz unity-gain frequency at room temperature.

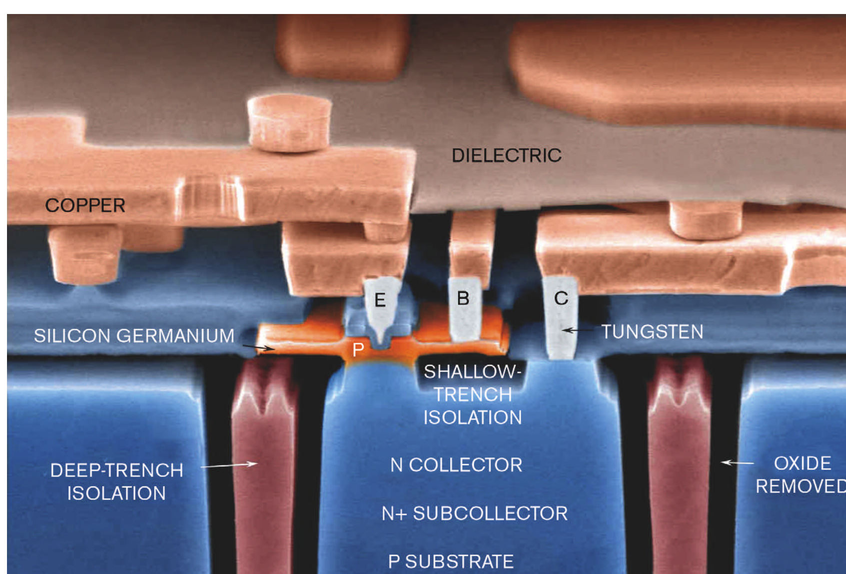
The HBT uses fundamental physics and quantum mechanics to achieve speeds in the hundreds of gigahertz. CMOS processes can achieve speed only by reducing device geometries, so operating voltages must be lower to prevent

breakdown across the transistors. For digital circuitry, that approach is acceptable because the transistors must convey only on and off states. But for analog, the SNR with this approach soon becomes unacceptable. To even approach 100 GHz, CMOS devices must decrease to sizes that will withstand a power-supply voltage of only 1V or less. "The real limitation of CMOS is the ever-dropping voltage," says Jean-Marc Mourant, senior scientist of IC design at Maxim Integrated Products. CMOS is the purview of low-performance applications in which cost and integration are primary, he says.

As the name *heterojunction* implies, the base of a SiGe transistor is the area that combines silicon and the germanium that an epitaxial reaction deposits. If you want to add SiGe to a CMOS line, you have to purchase only one epitaxial reactor, and the rest of the fab flow remains the same. The germanium in the silicon lattice provides far more benefits to a bipolar transistor than it does to the germanium-implanted channel of a strained-silicon-CMOS process. Like with the strained silicon, the mobility increases, but you derive more benefit from the change in the bandgap. For this reason, HBT processes benefit from bandgap engineering.

Germanium allows higher dopant concentrations in the base region. "You are lowering the base resistance without killing the current gain," says Derek Kimpton, parasitics-product-line manager at TCAD-simulation-software manufacturer Silvaco. "The lower base resistance of the SiGe HBT also has the added benefit of creating a low-noise device, an important criterion for RF-circuit designers." The whole idea behind SiGe, like any other HBT, is that you can use more dopant for the base because a bandgap exists between the base and the emitter, so emitter-injection efficiency remains stable, according to Robb Johnson, PhD, director of technology at fabless-components company Inphi. "You can dope the base higher without killing the device performance, and, at the same time, you can make the base narrower and speed up the transit time," he says.

Using SiGe also increases the f_T, the unity-gain frequency of a transistor's short-circuit current gain. The doping concentration creates a field that accelerates the electrons in the devices (**Figure 5**). In a conventional silicon transistor, higher doping would lower the current gain and allow leakage back to the collector. In a SiGe transistor, the bandgap potentials maximize the current



NOTES: E=CONTACT TO EMITTER, B=CONTACT TO BASE, AND C=CONTACT TO COLLECTOR.

Figure 4 After dielectric etching, a color-enhanced micrograph of a SiGe transistor showcases the device. A real device has no air or vacuum between regions (courtesy Subramanian S Iyer, IBM).

gain and minimize leakage. The higher dopant concentration makes the silicon act more like a metal and less like an insulator. The base is more conductive, and the base resistance decreases, making the noise factor in SiGe transistors better than that of pure-silicon devices. As with all other analog processes, however, you must make trade-offs: lower emitter resistance or reduced leakage, for example. You achieve all these performance enhancements on a process line that differs little from that of any other silicon fab.

"If you increase the base dopant in a regular transistor, you can reduce the base resistance and improve the Early voltage, but you usually kill the current gain," says Marco Corsi, a fellow at Texas Instruments. *Early voltage* takes its name from its discoverer, US engineer James M Early. The Early Effect is the variation in the width of the base in a BJT (bipolar-junction transistor) due to a variation in the applied base-to-collector voltage. "You can't run the transistor at high current density if you don't have any current gain," says Corsi. "The SiGe improves the current gain, which allows you to run higher base dopings."

Mike Maida, National Semiconductor's chief technologist, adds: "By putting germanium into the silicon, you get a variable bandgap as a function of distance. This [approach] gives you another handle to tweak the current gain." According to Maida, you needn't trade off current gain versus base resistance. The thermal noise of the base resistance appears as a noise term, and higher base resistance also degrades the maximum frequency. Brad Scharf, a fellow at Analog Devices, explains that factors that decrease base resistance also derive from factors such as geometry shrinkage that do not directly relate to adding germanium. "The beta Early-voltage product is also an indication that the base resistance in the transistor is

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lower with SiGe than it would be in an otherwise-comparable silicon transistor," says Scharf.

All of these benefits yield better transistors, according to David Harame, a fellow and director of derivative- and value-added-technology development at IBM. Developers of HBTs build the devices vertically, whereas CMOS' developers base the devices on lateral scaling and lithography. "The SiGe allows you to improve the overall figure of merit," says TI's Corsi. "Particularly with the PNP, it allows you to make the transis-

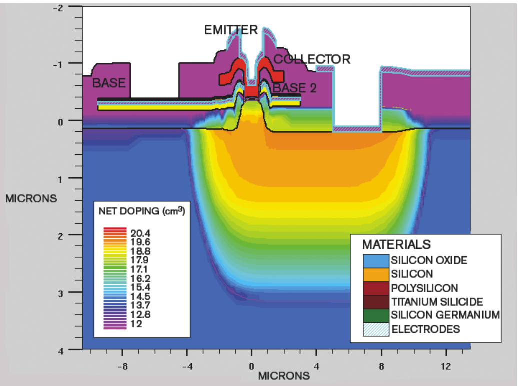

Figure 5 Varying the doping concentration across the base of a SiGe transistor creates an electric field that accelerates the electrons and speeds up the device (courtesy Silvaco).

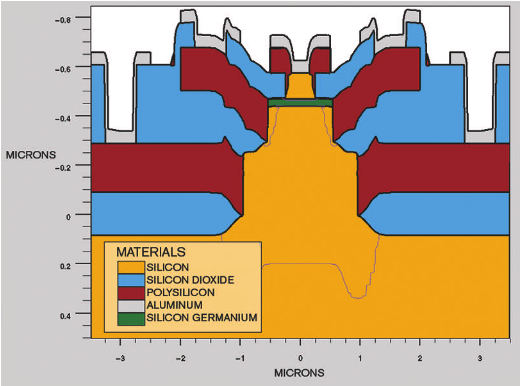

Figure 6 By modeling the physical transistor, a CAD tool can help derive design rules and device characteristics (courtesy Silvaco).

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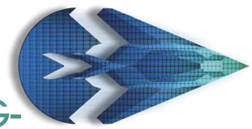
tor much closer to the performance of the NPN. This … symmetrical process is great for building amplifiers and linear circuits." In short, using SiGe processes yields speed, along with low noise, higher voltage, lower power, and all the further benefits of the improved specs.

NO ROSE-COLORED GLASSES

Not everything in the SiGe world is perfect. Almost every analog-semiconductor company has a horror story about moving a process from one fab to another and losing the process, sometimes for years. Adding a machine cannot reduce capitol costs or improve yield. "The fact that you have more process steps has to hurt the yield; 10% more process steps automatically give you a few percentage points less yield," says Artur Balasinski, process-technology-development-engineering manager at Cypress Semiconductor. BiCMOS SiGe involves other cost implications, as well. Because the BiCMOS processes have wider lines and larger geometries, the dice are larger than those using the latest CMOS processes. And, even though the BiCMOS mask set is cheaper, the process makes little sense for high-volume parts with predominantly digital content. "Going back two generations to implement something that is merely 'faster' but doesn't provide you with much other competitive advantage and is also faster in a domain that you may not care about much makes BiCMOS a hard sell," says Balasinski.

The trade-offs favoring SiGe depend on each company's experience, capabilities, and strategy. National Semiconductor's use of SiGe BiCMOS in its interface parts makes sense because a serializer or a deserializer needs a handful of fast transistors to handle the 5- or 10-Gbps serial-data stream, which is an analog signal. Once inside the chip, the parallel-data flow runs at speeds that conventional CMOS can handle. Because these parts have few digital-processing needs, the benefits of SiGe outweigh the geometry hit of a BiCMOS process.

An advantage of SiGe models is that they can work with available tools. "Models for analog devices require a high degree of sophistication," says Subramanian S Iyer, a distinguished engineer and chief technologist at IBM. "A bipolar transistor definitely has a more complex model. We have [provided]



ALMOST EVERY ANALOG-SEMICONDUCTOR COMPANY HAS A HORROR STORY ABOUT MOVING A PROCESS FROM ONE FAB TO ANOTHER AND LOSING THE PROCESS, SOMETIMES FOR YEARS.

and will continue to provide a robust, accurate model. We have been so successful in our analog- and mixed-signal effort [because of the] attention we have paid to generating, testing, and verifying these models."

This observation does not dismiss the issues of adding bipolar SiGe to a CMOS flow, however. "With CMOS, you have a limited number of device models," says Cypress' Balasinski. "You have a particular number of transistors, and interpolation doesn't always work. More often than not, for analog you have discrete models. If you throw in the modeling complexity of BiCMOS, then it kind of kills you right away because you have so much more to maintain to build similar kinds of devices. You have 20 to 50 transistor models, and this number then doubles because you have to have a model for each variation of a bipolar transistor." Calibrating, developing, maintaining, verifying, and testing these models; keeping the line up for model validity; and ensuring that the models don't diverge take a lot of effort, he notes. Getting those models into a product is even more work. For example, you may want to transfer your models to TSMC (Taiwan Semiconductor Manufacturing Co). "You can have them copy exactly, but [TSMC] needs to keep track of your models, and matching them is no small task because the company may have totally different tool sets." Further complicating these issues, all analog processes are highly sensitive to change. "We are talking about subtle things that may work in one fab and not in another," he says.

The same situation holds true for strained silicon in CMOS: "In general, selective SiGe is a sensitive process," says Sri Samavedam, manager of 32-nm bulk integration at Freescale Semiconductor. "Any time you tweak or make any process change you have to recharacterize all the parameters."

Marc Goldfarb, a design engineer with Analog Devices, points out that trench and dielectric isolation also affects the models, meaning that you must consider thermal effects. "Trench and dielectric isolation result in slightly different thermal profiles," he says.

The need for sophisticated tools is not so much a function of the SiGe itself as the fact that, if you are using SiGe, you are probably designing a high-performance IC that needs sophisticated tools to ensure that the part will work properly. SiGe models can plug into midrange Spice tools, such as Cadence/Orcad's PSpice, as well as Synopsys' industry-standard HSpice. SiGe ICs most likely operate at nearly RF frequencies, however, so it also makes sense to have a field solver in the tool flow to ensure that crosstalk and interactions between circuits are not objectionable (**Reference 4**). In addition, fast chips are incorporating spiral inductors to make tank circuits. You may also want a tool set that can do the physics modeling, which helps you establish design rules so that your device behaves as it should after layout. "We are using a computational grid—a mesh," says Synopsys' Borge. "On that grid, we are solving the semiconductor equations. It is first-principle physics, and, more recently, we have had to include quantum-mechanical effects, particularly for the channels in the PMOS devices." Full-featured SiGe tools include a Spice engine, a field solver for the RF, and a physics modeler for the transistors (**Figure 6**).

The future of SiGe is good in view of its main competition, the III-V semiconductors, including gallium arsenide and indium phosphide. Although III-V compounds are even faster than SiGe, they are also more costly. Worse yet, the lack of an effective oxide layer in III-V semiconductors makes them less appealing for integration of entire subsystems on a die. Furthermore, the fabs that make these ICs all have smaller wafers; 6-in. wafers are common. The specialized needs of these devices mean that you cannot fabricate them on any variant of a CMOS-fab flow. SiGe's benefits really pay off in RF amplifiers. "SiGe RF-power amps have a big advantage," says National Semiconductor's Maida. "You can integrate them with CMOS so you no longer need an expensive, esoteric, gallium-arsenide die that sits by itself."EDN

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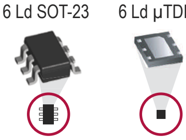

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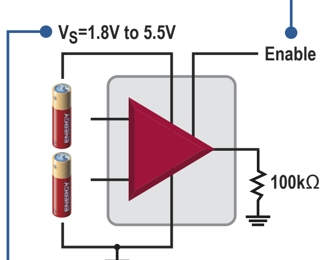

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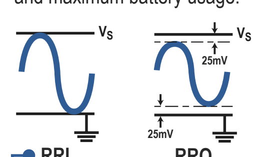

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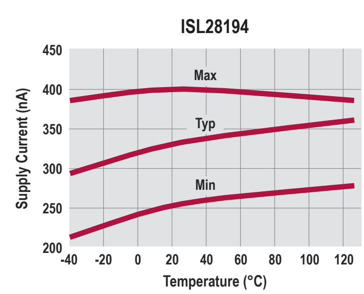

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DISPLAYPORT VERSUS HDMI: Do we really need two digital-display-interface standards?

DisplayPort proponents bill this digital-video-I/O standard as a no-royalties, scalable, extensible, open-standard interface that reduces connector footprint and cable clutter, lowers power consumption and cost, eliminates the need for some circuitry, and unifies interfaces in the boxes that connect to the home network. VESA (Video Electronics Standards Association), which introduced DisplayPort in 2006, last year ratified DisplayPort version 1.1a. Silicon is beginning to appear in PCs, LCD monitors, and cable assemblies, as well as in some motherboards and graphics cards. PC makers initially developed DisplayPort to address computing-world concerns and replace the external, box-to-box, analog-VGA (video-graphics-array) interfaces in PC and LCD monitors, as well as in CE (consumer-electronics) equipment, but it also targets the external DVI (digital-visual-interface) connectors you find mostly in CE systems. It even promises to replace the internal, board-to-display, LVDS (low-voltage-differential-signaling) links in both PC and CE devices.

During the past couple of years, however, while VESA was hashing out the standard and getting working DisplayPort chips and systems operating and certified, manufacturers began shipping high volumes of silicon for the older, external-only, HDMI (high-definition-multimedia-interface) digital-video-interface standard. The designers of HDMI created it to replace DVI and based it on DVI's legacy raster-scan CRT architecture. Despite the $5000 to $10,000 annual fee and royalty structure of 4 cents per device, HDMI ports now see use in several hundred million digital TVs and other CE equipment that incorporates digital video, such as game consoles, DVD (digital-video-disc) players, Blu-ray-disc players, and digital-set-top boxes. Perhaps more important to DisplayPort supporters, HDMI has also begun to appear in graphics cards, PCs, and monitors to enable connectivity to HDTVs (high-definition televisions).

According to Brian O'Rourke, principal analyst for In-Stat, although manufacturers will ship limited amounts of DisplayPort-enabled products during 2008, shipments will grow to more than 600 million units in 2012. Most of these shipments will be PCs and PC peripherals (**Figure 1**). "I don't see DisplayPort really gaining significant market share in the consumer-electronics world in the next five years," says O'Rourke. "During that time, it will dominate the PC and PC-peripheral world, and HDMI will dominate the consumer-electronics world. HDMI has buy-in from the big consumer-electronics manufacturers, and they tend to be conservative. The key for DisplayPort in the PC segment is that you can get rid of both the DVI controller and the VGA silicon." In 2007, manufacturers included DVI in 13% of desktop PCs, 28% of desktop PC monitors, about 16% of LCD-notebook-PC monitors, and all after-market graphics cards.

One reason HDMI ports are growing so fast is the increasing port density in PC displays and TV monitors, says Randy Lawson, iSuppli's senior analyst for display electronics. Multifunction PC monitors are becoming more common, typically with two ports, and HDMI is replacing the old DVI port. "Some PC-flat-panel-monitor makers are very pro-HDMI, especially outside the U.S., where people often use their PC monitors as displays for video," says Lawson. "Perhaps surprisingly, this is one area where there will be real competition between HDMI and DisplayPort." In fact, iSuppli expects HDMI's adoption rate in PC monitors to outpace DisplayPort's until 2010, when DisplayPort will dominate desktop and notebook PCs. To some extent, this situation will also occur because of the higher initial cost

DISPLAYPORT SILICON IS BEGINNING TO APPEAR IN PCs, LCD MONITORS, AND GRAPHICS CARDS. BUT IT WILL PROBABLY BE AT LEAST FIVE YEARS BEFORE PRICES FALL AND VOLUMES RAMP ENOUGH TO CHALLENGE HDMI IN CONSUMER ELECTRONICS.

of first-generation DisplayPort silicon. The HDMI-enabled-equipment market will expand even more as designers of additional consumer equipment, such as high-definition camcorders and video-game consoles, move to support high-definition video.

DIGITAL AUDIO/VIDEO AT HOME

This competition is heating up because the proliferation and distribution of digital-video and -audio content are driving product development in both computing and CE, as well as in communications, and they're all converging in the home network. There's also the advent of high-definition video and content-protection and DRM (digital-rights-management) issues.

The developers of the HDMI standard, now in its fourth generation, designed it primarily as an external interface for digital TVs, especially HDTVs. DisplayPort's developers designed it from the ground up as a general-purpose internal and external display interface for computing equipment. Both standards digitize analog-video signals but in different ways (**Table 1**, available in the Web version of this article at www.edn.com/080918cs). Because HDMI's designers based its raster-scan architecture on the serial-TMDS (transition-minimized-differential-signaling) protocol, it sends each color over a separate data channel, plus another lane for the dedicated TMDS clock. Therefore, it always requires the use of all four lanes. Audio transfers occur during horizontal- and vertical-display-blanking periods. HDMI also uses two additional channels: a bidirectional auxiliary-control/status channel, and a high-level device-control channel. For DRM, it relies on the HDCP (high-bandwidth-digital-content-protection) scheme, currently HDCP 1.3.

In contrast, DisplayPort combines audio, video, and control data into packets, such as those in data networks. This packet-based architecture lets you use one, two, or four data channels to trade off screen resolution, pixel depth, frame rate, and additional data, such as audio or DRM information. A 1-Mbps, bidirectional auxiliary channel provides link management and device control. DisplayPort's embedded clock eliminates the need for extra circuitry and streamlines its already-scalable design, making it easier for designers to increase data rates in the future. The embedded clock also helps avoid common frequency conflicts between an LVDS clock and other clock sources, such as radios.

Although DisplayPort supports content protection through the DPCP (DisplayPort Content Protection) encryption protocol, adopting the HDCP scheme, the standard does not require it. It does efficiently encrypt DisplayPort packets and the HDMI signal in one HDCP 1.3 block, says Pericom Semiconductor's Abdullah Raouf, product-marketing manager for switch and interface marketing and a member of VESA's DisplayPort Task Group. VESA anticipates that all consumer applications of DisplayPort will include content protection, which will require specifications and license agreements separate from the DisplayPort spec.

"The major advantage of DisplayPort's packet architecture is the variable possible number of wires in the cable," says Bruce Montag, chairman of the DisplayPort Task Group and senior technical-staff member at Dell. As notebook computers continue to get smaller, their display resolution and color-bit depth increase, and designers add communication capabilities by routing antennas through the notebook's hinge, where reducing the number of wires becomes a primary concern. DisplayPort enables thinner, smaller-form-factor monitors because the signal can go directly from the PC to the glass in the monitor in direct-drive, end-to-end configurations that replace LVDS with DisplayPort. In addition, the LVDS auxiliary channel is one-way, whereas DisplayPort's bidirectional channel provides the ability to perform additional functions, such as notebook-backlight control.

Direct-drive monitors that remove the scalar from the mix can save 15 to 20% in overall monitor BOM (bill-of-materials) costs, including the PCB (printed-

AT A GLANCE

- VESA (Video Electronics Standards Association) finalized the DisplayPort digital-video-I/O specification in April 2007, and silicon has appeared this year in PCs, LCD monitors, and cable assemblies, as well as in some motherboards and graphics cards.
- Products employing DisplayPort include Lenovo's ThinkPad, Hewlett-Packard's DreamColor LCD monitor, several AMD ATI graphics cards, AMD's 780G chip set, and Intel's 45 Express chip set for Centrino 2.
- The HDMI (high-definition-multimedia-interface) standard has more than 800 adopters, and shipments of HDMI-enabled units reached 192 million in 2007.
- Semiconductor analysts are relatively bullish on DisplayPort's ability to penetrate PC-system markets, but whether and to what extent it can also make its mark in CE (consumer-electronics) equipment remains to be seen.

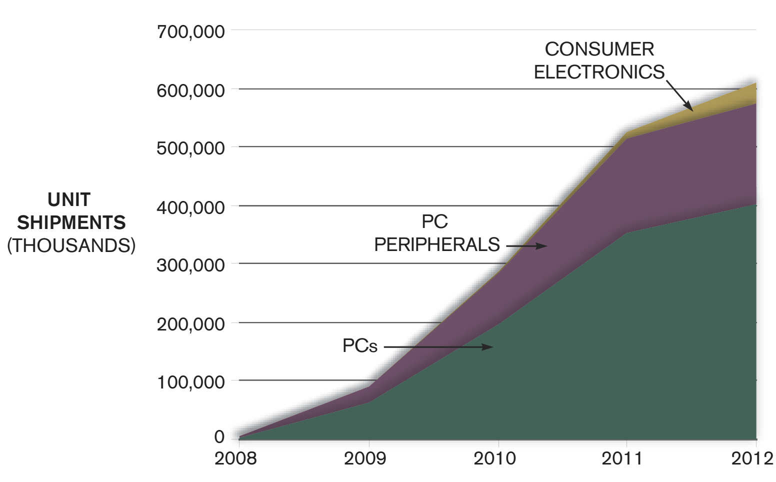

Figure 1 Total DisplayPort-enabled device shipments will grow to just over 600 million in 2012 (courtesy In-Stat).

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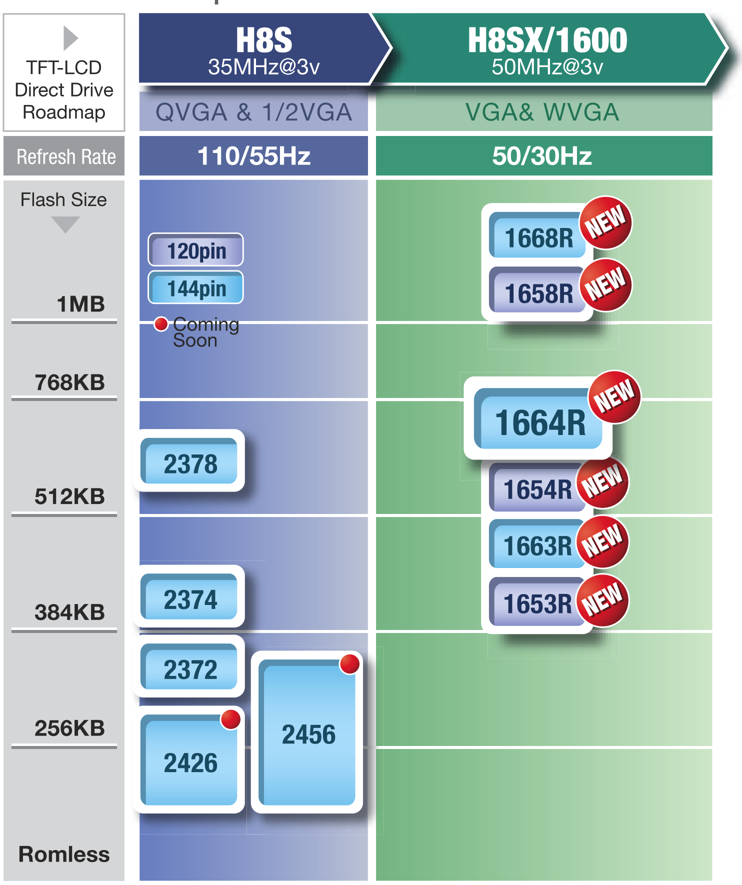

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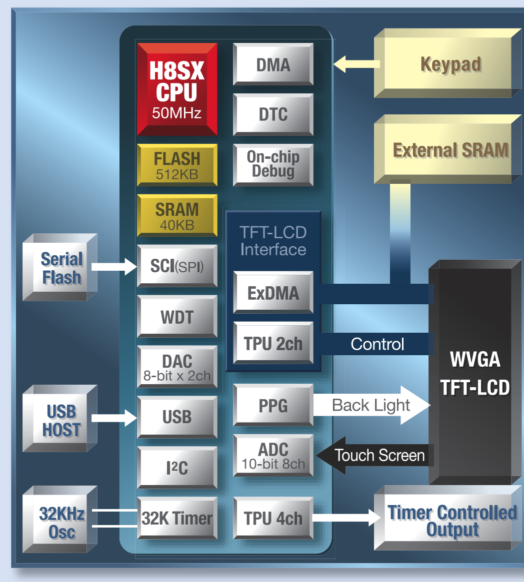

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circuit board), processor, capacitors, and resistors, says Ji Park, vice president and general manager of the digital-display operation of IDT (Integrated Device Technology). It also means an opportunity to integrate the display's timing controller with the DisplayPort receiver, as IDT has done in its PanelPort timing-controller silicon, which targets monitor, notebook, and LCD-HDTV panels.

Even without also replacing the external video interface, however, DisplayPort's potential for replacing the embedded, multipin internal LVDS interface in an LCD panel may hold the key to the standard's market penetration, especially in notebook PCs and LCD TVs, says iSuppli's Lawson. The company forecasts shipments of more than 600 million mobile PCs and 550 million LCD TVs between 2008 and 2011.

DISPLAYPORT-SILICON ISSUES

As process geometries get smaller, DisplayPort is also easier than HDMI to integrate and implement in silicon. Alan Kobayashi, director of R&D for the DisplayPort/TV/monitor division of STMicroelectronics' home-entertainment and displays group, wrote the original draft of the DisplayPort spec during his tenure with Genesis Microchip, which STMicroelectronics recently acquired. "Although LVDS is very well-accepted in the industry, as semiconductor processes shrink, it's not the most optimal technology," he says. For LVDS to handle 1920×1200-pixel resolution and 8 bits per color, it needs 10 high-speed

INTEROPERABILITY AND BACKWARD-COMPATIBILITY ISSUES

To ensure interoperability among devices from multiple vendors that contain external DisplayPort interfaces, VESA (Video Electronics Standards Association) has instituted a DisplayPort-compliance, -testing, and -certification program. You can now connect DisplayPort-enabled boxes compliant with multimode DisplayPort to other display interfaces in current or legacy TVs and other PC or CE (consumer-electronics) equipment through adapters, or dongles (Figure A). The VESA DisplayPort Interoperability Guidelines, which the association released in 2007, address DisplayPort-to-DVI (digital-visual-interface) and DisplayPort-to-HDMI (high-definition-multimedia-interface) adapters. VESA is working on other types of adapters, such as DisplayPort-to-VGA (video-graphics array), and is evaluating the need to certify embedded implementations of the spec.

"DisplayPort has been designed with backward compatibility in mind," says Devang Sachdev, Nvidia's technical-marketing manager and a member of the VESA board of directors. "There's already a large installed base for VGA and DVI, and these interfaces will be around for quite some time. That's why the DisplayPort standard

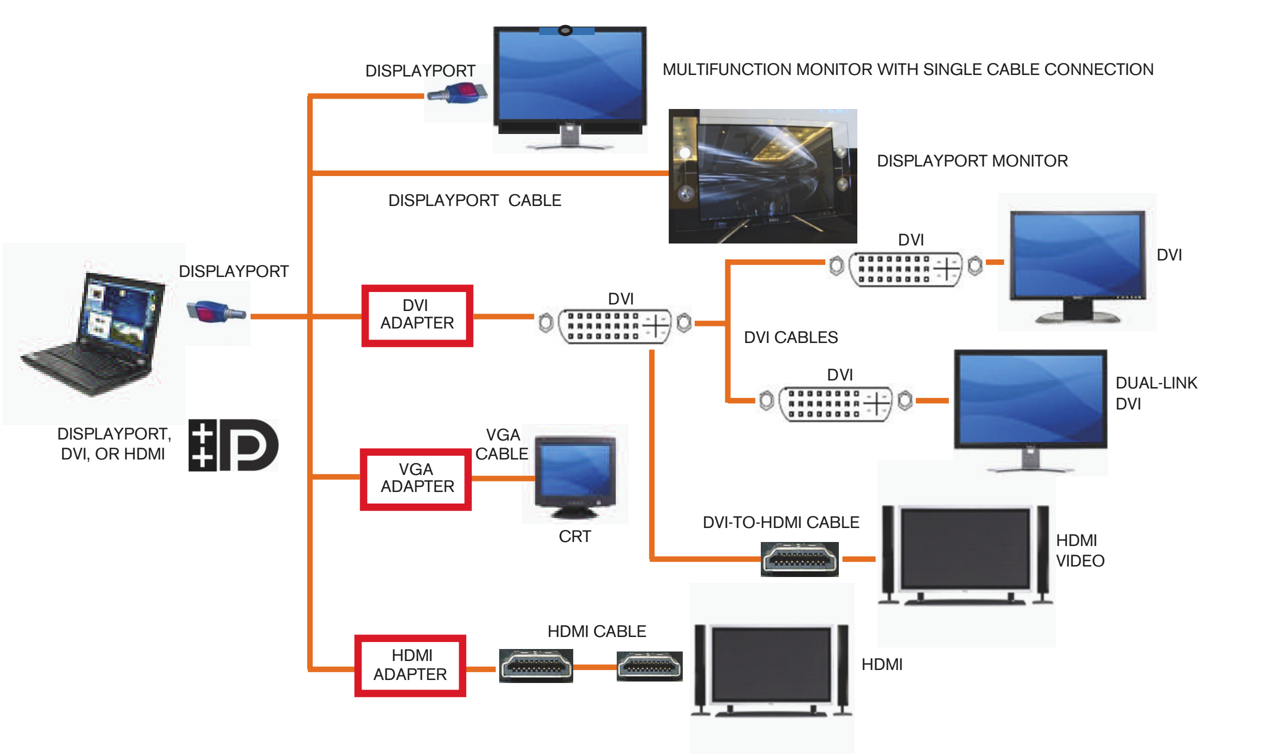

Figure A VESA DisplayPort-multimode-interoperability guidelines enable connectivity to other display interfaces (courtesy Video Electronics Standards Association).

differential-signal pairs, or 20 wires. For the same function, DisplayPort reduces this requirement to only two pairs, or four wires. An LVDS implementation requires at least 3.3 or 2.5V, so it's becoming increasingly difficult at 45-nm and smaller process geometries.

Because DisplayPort is ac-coupled, instead of dc-coupled like HDMI, it has a lower voltage swing and a different termination scheme. You must terminate HDMI only at the receiver and pull it up to 3.3V, says Pericom's Raouf. But you can terminate DisplayPort at both the source and the receiver, and it can never exceed 2V, per the spec, helping to lower power consumption. HDMI's I/O-voltage limitation becomes more of a constraint with shrinking process geometries, increasing cost and die size. DisplayPort's lower voltage swing also helps reduce EMI (electromagnetic interference).

DisplayPort transmitters are in all of the newer north-bridge chip sets' integrated graphics, as well as in discrete GPUs (graphics-processing units) on graphics cards, according to VESA's Montag. "Older GPUs can use a discrete DisplayPort-transmitter chip, but the need for that [part] is diminishing," he says. Although vendors such as Analogix Semiconductor and STMicroelectronics will offer discrete DisplayPort silicon in 2008, "the market is quickly moving toward the integration of DisplayPort IP [intellectual property] into a north-bridge or a discrete-graphics solution," says In-Stat's O'Rourke.

Intel and AMD have announced support for both DisplayPort and HDMI in chip sets for some of their latest processors: Intel's 45 Express chip set for Centrino 2 and AMD's 780G chip set. "Our next-generation discrete GPUs, as well as motherboard GPUs, will support a myriad of connectivity options, including HDMI, DVI, VGA, and, of course, DisplayPort," says Devang Sachdev, Nvidia's technical-marketing manager and a member of the VESA board of directors. "This [approach] affords our partners and customers the greatest flexibility."

DUAL STANDARDS, MARKETS

HDMI's presence in notebook computers and in TVs and other CE equipment means that HDMI is quickly becoming the method of convergence. Although consumers may be converging PC and CE equipment in their own home networks, however, many manufacturers see the two as separate markets. DisplayPort backers now talk about coexistence, with HDMI leading in CE and DisplayPort leading in PCs (see **sidebar** "Interoperability and backward-compatibility issues"). In the early days of the spec's development, however, the debate was more heated. In particular, some suppliers of HDMI silicon for the CE market, especially for large digital-TV OEMs, see little value in DisplayPort.

New consumer features should differentiate DisplayPort from HDMI, says Doug Bartow, strategic-marketing manager for the advanced-TV segment at Analog Devices, who participated in DisplayPort standards development. "In our view, there are no consumer features in DisplayPort that distinguish it over HDMI," he says. "As an engineer, I think that DisplayPort is a well-constructed display standard, and, if it were available three to four years ago, we'd all be using

enables interoperability between DisplayPort-capable devices and DVI/HDMI-capable devices through the use of adapters," he says.

The DVI and HDMI adapters include a chip that performs voltage-level shifting but does not perform format conversion from DisplayPort to DVI or HDMI, says Bruce Montag, chairman of VESA's DisplayPort Task Group and senior technical-staff member at Dell. The adapters don't need to perform format conversion because multimode DisplayPort GPUs (graphics-processing units), which also support DVI/HDMI signaling, detect the presence of these adapters and transmit signals in the format compatible with the display to which they connect. This ability is key for systems, such as ultrathin notebook computers, that have enough space for only one display connector but must connect to a variety of displays.

Voltage-level-shifting chips, which run on power from the DisplayPort connector's power pin, are available from vendors such as Pericom Semiconductor. Pericom's chips provide the electrical bridge that converts the low-swing, ac-coupled DisplayPort signal to the dc-coupled TMDS (transition-minimized-differential signaling) that HDMI and DVI use. They also include a circuit to eliminate jitter, which increases with rising transmission speeds, says Abdullah Raouf, Pericom's product-marketing manager for switch and interface marketing.

DisplayPort also supports longer cables than most available today for DVI or HDMI—as long as 15m for a source and a display that are both DisplayPort-compliant. This capability is important for several uses, such as digital projectors. The connector is latchable to avoid cable falloff, which can occur with heavier cables. Although DisplayPort runs over Category 5 cable, HDMI requires the more expensive Category 2 type. However, other options include cables equipped with Gennum's ActiveConnect-receiver silicon, which enable reaches as long as 100m at maximum bandwidth for either HDMI or DisplayPort.

One of HDMI's major shortfalls is its inability to daisy-chain multiple monitors in a single HDMI connection—the fault of its TMDS protocol, says Ji Park, vice president and general manager of the digital-display operation of IDT (Integrated Device Technology). Therefore, you need multiple graphics cards for multiple monitors, he says. "But DisplayPort's extensible architecture lets you assign each monitor a certain address or a certain lane and hence support multiple monitors with a single source device."

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it. But HDMI is already here, and it will provide significant headwinds for market penetration of DisplayPort." Analog Devices makes silicon for DVI, VGA, and HDMI for the top 20 TV manufacturers. Although the company has implemented DisplayPort test chips, it has found insufficient demand from customers to fund the chip development, adds Barstow.

The need for systems and silicon that deliver digital content is growing even beyond the traditional home network, at least on the CE end. "There's been a big switch out there in the manner of delivering digital content," says Dale Zimmerman, vice president of worldwide marketing for Silicon Image. The company co-founded the HDMI specification, manufactures HDMI silicon, and licenses HDMI cores under its wholly owned subsidiary, HDMI Licensing. This explosion has happened for a number of reasons, he says. In particular, there are multiple sources of digital-video content and broadening distribution channels for delivering it. For example, one of the newest content sources is the mobile phone, and far more people own one of these devices than own a PC.

The size of the CE market is several times that of the PC market; there are more types of boxes, and many more people have them. Adding mobile devices could double the size of that market. "CE manufacturers are not interested in another standard or another connector on the back of the TV," says Zimmerman. Silicon Image has announced product development for mobile-high-definition-link chips that address PDAs (personal digital assitants) and mobile phones. But VESA has not yet finalized the mobile-display-digital-interface standard for external DisplayPort-display connectivity to cell phones and other portable devices.

Although DisplayPort's potential in the CE market is less certain than its future in the PC market, there's some opportunity for replacement of the high-pin-count connectors that connect digital-TV boards to panels inside the TV, says In-Stat's O'Rourke. "That doesn't necessarily mean there will also be DisplayPort ports on the outside of those TVs," he says. "Still, that's a foot in the door, a Trojan horse, for DisplayPort. If you're in the digital TV, you're in the center of the living room." In-Stat expects that, by 2009, digital TVs will begin adopting DisplayPort as an internal feature, resulting in its appearance in some external ports, especially in higher-end digital TVs, the following year. DisplayPort ports will then be able to migrate to other digital-CE products, including Blu-ray players and recorders and set-top boxes. EDN

> **+ For an analysis of DisplayPort's partitioning and how it differs from TMDS-based architectures, see www.edn.com/article/CA6574650.**
>
> **+ For details on how display interfaces work, as well as a discussion of the history and politics behind the development of the DisplayPort and HDMI standards, go to www.edn.com/article/CA6402885.**
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AUTHOR'S BIOGRAPHY

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BY ERIC BOGATIN, PHD, BOGATIN ENTERPRISES • BILL HARGIN, MENTOR GRAPHICS

Making the transition from bit banger to gigabit guru

AS HIGH-SPEED SERIAL INTERCONNECTIONS INFILTRATE TECHNOLOGY, SYSTEM DESIGNERS FACE A SERIES OF NEW SIGNAL-INTEGRITY PROBLEMS TO MANAGE.

Interconnects are not "transparent" to digital signals and haven't been for more than 25 years—since the end of the 20-MHz-clock-frequency regime. High-speed onboard buses drove the lexicon of signal integrity into the vocabulary of every board designer. For that reason, the design guidelines for digital products today all use controlled-impedance boards, terminate all lines, avoid branched routing topologies, reduce inductance of the return paths, and use low-impedance power- and ground-distribution networks.

In the last few years, the proliferation of high-speed serial links, such as PCIe (peripheral-component interconnect express), SATA (serial-advanced-technology attachment), and InfiniBand, has brought with it a new set of challenges that pushes designers into a new regime of signal-integrity problems. This article focuses on four critical problems that confront designers in this new world—frequency-dependent losses; impedance discontinuities, especially from surface pads and vias; intrapair skew; and channel-to-channel crosstalk—and a few tips and tools that will help alleviate some of the pain.

As bit rates increase, the option of relying on luck in the design process decreases proportionately. Successful high-speed-serial-link design must now recognize these problems and leverage the design, materials, and technology approaches to eliminate them right from the start.

The bandwidth of a high-speed serial link, the highest sine-wave-frequency component in the signal, can be as high as 2.5 times the bit rate, which corresponds to the fifth harmonic of the highest bit-transition rate. For example, a PCIe Generation 2 signal at 5 Gbps can have a bandwidth as high as 12.5 GHz. At these frequencies, the interconnects themselves cause four special problems that you must avoid to navigate safe passage.

The first step in avoiding these problems is to recognize them. The second step is to identify their root cause and establish design guidelines to avoid or minimize them. Although design guidelines tell which knobs to tweak and in which direction, an accurate simulation tool that includes these effects is essential to navigating safe passage through design, balancing the trade-offs between cost and performance gain, and meeting acceptable performance specs.

FREQUENCY-DEPENDENT LOSS

As a signal propagates down a board trace, frequency-dependent losses from the conductor and dielectric materials attenuate higher-frequency components more than lower-frequency components. Skin-depth effects constrict the cross section of the trace through which current flows, increasing the series resistance of both the signal and the return paths. This series resistance increases proportionally to the square root of frequency. The motion of dipoles in the dielectric material causes a

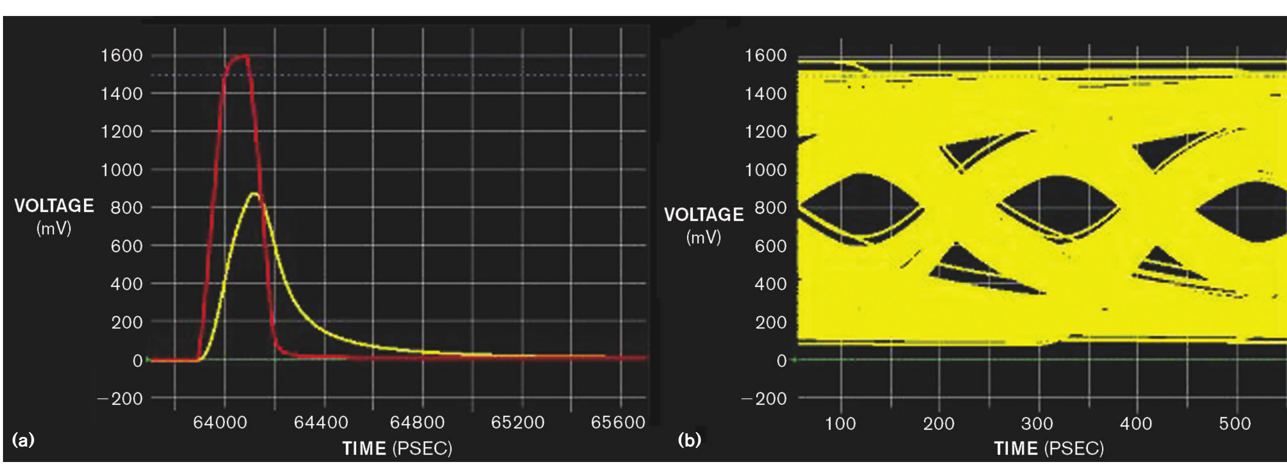

Figure 1 The 200-psec-long single-bit response shows the incident bit in red and the same bit in yellow after 30 in. of FR4. The spreading of the bit causes intersymbol interference (a). Mentor Graphics HyperLynx simulates the resulting eye diagram of a 5-Gbps pseudorandom-bit-sequence signal (b).

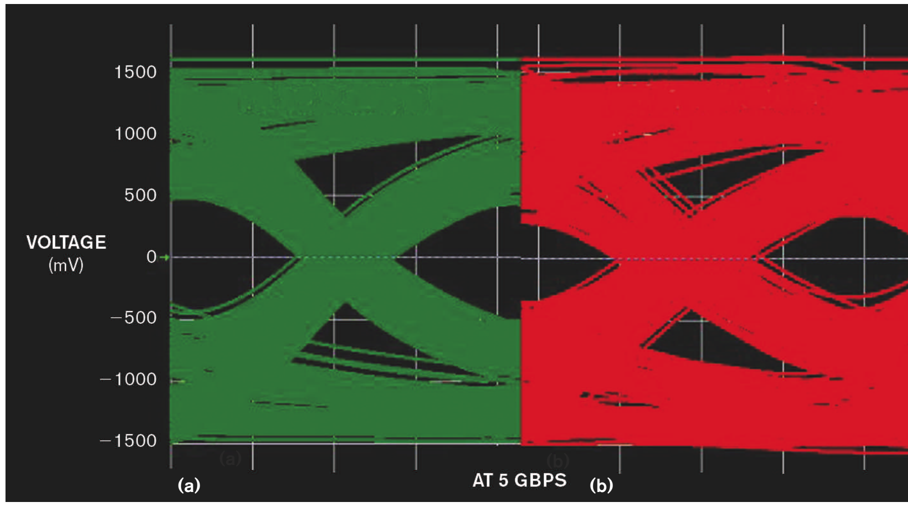

Figure 2 HyperLynx simulates an eye diagram of a backplane interconnect without via stubs (a) and with via stubs (b), approximately 200 mils long.

leakage current between the signal and the return paths that increases proportionally to the frequency. As the dipoles rotate in the electric field of the signal, the leakage current and the associated loss increase proportionally to frequency.

Both of these effects contribute to higher frequencies seeing more attenuation than low frequencies. As a fast-rising edge propagates down the line, fewer high-frequency components remain in the signal, and the rise time increases. This rise-time degradation is the chief cause of ISI (intersymbol interference), which results in the collapse of the eye and deterministic jitter. For example, the losses in a 30-in.-long, 5-mil-wide, 100Ω differential pair in FR4 dramatically degrade the rise time of a PCIe Generation 2 signal at 5 Gbps. One bit affects the next bit so much that the eye nearly closes (**Figure 1**).

Unfortunately, you have only two design knobs to tweak to improve the performance: Increase the line width of the traces and increase the dielectric thickness to preserve the 100Ω impedance or use a laminate material with a lower dissipation factor than FR4. You should also consider decreasing the interconnect length, but this approach is rarely an option.

If conductor and dielectric losses, which increase monotonically with frequency, dominate the rise-time degradation, two important signal-processing techniques can bring back the original shape of the signal's spectrum. If the problem is losses at higher frequency, then add pre-emphasis—that is, extra high frequency to the original signal. Alternatively, you can use de-emphasis—removing some of the transmitter's low-frequency components. De-emphasis consumes less power and has less impact on crosstalk than does pre-emphasis.

Finally, if you know the transfer function of the interconnect, you can employ equalization—adding frequency-dependent gain at the receiver to balance the losses in the line. The combination of pre-emphasis or de-emphasis and equalization can extend the life of low-cost FR4 boards with narrow lines. These signal-processing techniques can overcome even −30 dB of frequency-dependent attenuation.

IMPEDANCE DISCONTINUES

The signal propagating down an interconnect sees an instantaneous impedance each step along its way. When this instantaneous impedance changes, some of the signal reflects, and the transmitted signal distorts. With multiple discontinui-

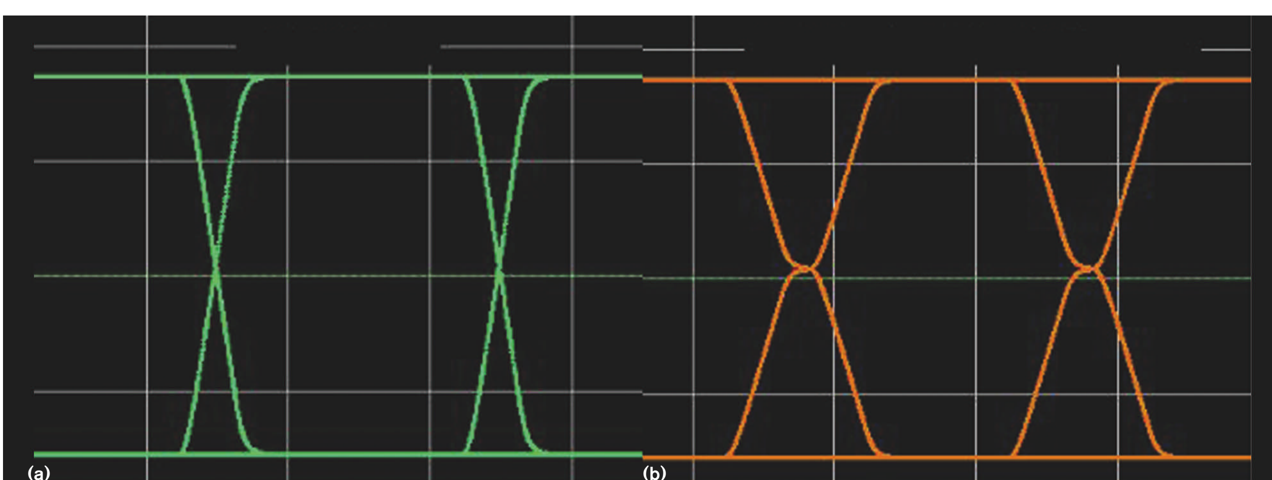

Figure 3 HyperLynx simulates an eye diagram of a transmitting signal with no skew (a) and with a skew 1.5 times the rise time of a 5-Gbps signal (b).

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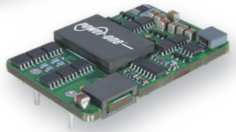

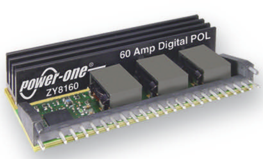

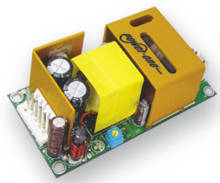

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ties, the reflected echoes can reach the receiver and cause ISI. The solution to this problem is to minimize impedance discontinuities. Two structures create the biggest discontinuities: surface pads for dc-blocking capacitors and through-hole vias. The dc-blocking capacitors enable drivers with a large common signal level to interface with receivers that can't tolerate a dc offset. Any capacitance greater than approximately 1 nF is enough to keep the series impedance low. However, unless you take care, the mounting pads of the capacitor create an impedance discontinuity on the surface trace. The solution is to use the smallest body-size capacitor you can afford, such as an 0402, and to reduce the size of the pads to the minimum acceptable for assembly operations. In some cases, removing the plane underneath the pads and capacitor to create a "shadow" or "relief hole" in the plane can minimize the impedance discontinuity. This trick often matches the impedance of the pads and capacitance to the 50Ω of the surface trace.

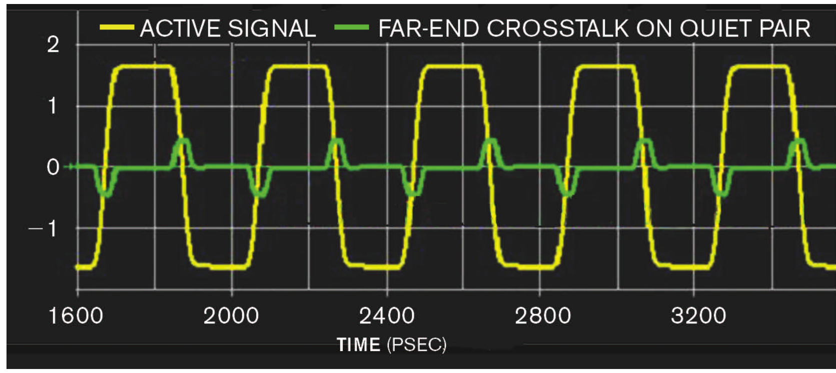

Figure 4 Received differential signals on adjacent, 19-in.-long, differential pair microstrips show far-end noise on the quiet channel, with 5-mil lines and spaces per pair and 10-mil spaces between the pairs at 5 Gbps (simulated with HyperLynx).

The impedance discontinuity of a through-hole via is a more insidious problem. With through-hole technology, a barrel through the entire board connects any two signal lines on different layers. If the layers are buried in the middle of the board, the barrels above and below the signal layers act as stubs. If the stubs are shorter than approximately 50 mils, they look capacitive and slow down the edge of the signal, causing rise-time degradation and ISI. If they are longer than 50 mils, they may act as resonators and cause excessive scattering of signals at or near the resonant frequency. A stub that is 200 mils long has a resonant frequency of approximately 7.5 GHz—well within the 12.5-GHz bandwidth of a PCIe Generation 2 signal (**Figure 2**).

You can combine design and technology to address via discontinuities. The first step is to minimize the capacitance of vias by removing nonfunctional pads on inner layers, increasing the antipad clearance holes, and minimizing the size of capture pads on the surfaces and on signal layers. You can minimize stub lengths by restricting layer transitions and minimizing the total board thickness. If the stubs are still excessively large, backdrilling can remove the residual barrel. Alternatively, you can implement other via technologies that do not create stubs. These technologies include blind or buried vias and high-density-interconnect microvias that you fabricate by laser drilling. These microvias are the shortest, lowest-capacitance, and most transparent vias available.

INTRAPAIR SKEW

All high-speed serial links use differential signals. Two independent signal paths carry each half of the differential signal. The pure differential signal from even the best driver can degrade into a common signal if any asymmetry exists between the two lines of the pair. The greatest source of asymmetry is time-delay skew between the two lines. The easiest way to minimize time-delay skew is to match the physical lengths of the two lines. If one line starts out a different length due to its escape or fan-out from a BGA-via field, for example, you should make the other line longer as soon after the via field as possible. Unfortunately, time-delay skew can arise from causes other than length. The local speed of the signal due to local variation in the dielectric constant of the resin-glass composite can also affect time-delay skew.

Weave-induced skew occurs when one line sees a different dielectric constant from the other line due to proximity to a glass-fiber bundle. The impact of weave-induced skew is roughly 0 to 10 psec/in. and depends on the chance alignment of one signal trace adjacent to a glass bundle. A 20-in. trace on a board could see a weave-induced skew of 10 to 100 psec. When the entire unit interval for a 5-Gbps signal is only 200 psec, any skew larger than 20 psec eats up the total skew margin and begins to degrade the eye diagram (**Figure 3**).

The easy approach is to match lengths between lines that make up a differential pair so that the time-delay skew is less than a few percentage points of the unit interval. The more-involved problem is minimizing the weave-induced skew. Techniques for addressing this skew include rotating the routing axis from the glass-weave axis, adding a small jog in traces longer than a few inches so that the two lines mix the local dielectric constant, and using a glass that either is more uniform or has a dielectric constant closer to the resin.

CHANNEL-TO-CHANNEL CROSSTALK

The bit pattern in adjacent channels is uncorrelated. Any signal from one channel that couples over to an adjacent channel therefore acts as random noise, collapsing the eye, increasing the crossover widths, and introducing random jitter. Differential crosstalk in connectors, in via fields, and between differential pairs is typically −35 dB or less. When the received signal is −10 dB, the margin is usually adequate, and crosstalk is not a problem. However, far-end crosstalk between adjacent mi-

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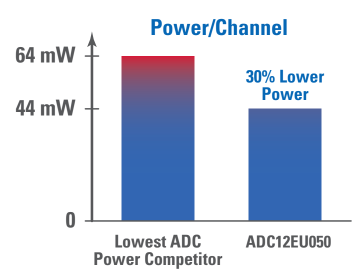

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crostrip-surface pairs can easily exceed −20 dB. For example, in two edge-coupled, differential microstrips with 5-mil lines and 5-mil spacing, a 10-mil pair-to-pair spacing, a 40-psec rise time, and a 5-Gbps signal, the far-end differential noise is almost −10 dB for a length of only 10 in. Because far-end noise is so sensitive to rise time and coupled length, a simulation is an essential step in evaluating the impact of far-end noise in microstrip-differential channels (**Figure 4**). Even near-end noise in stripline pairs can pose a problem under some cases. When the signal at the receiver decreases as a result of 30 dB of loss and when you use 10 dB of pre-emphasis on the transmitter, you must reduce crosstalk to less than −50 dB to provide adequate margin. You usually implement this reduction by using low-noise connectors and increasing the pair-to-pair spacing in the backplane.

Successful design and implementation of robust, high-speed serial systems are tricky because interconnects are not transparent to the signal. Unless you take special care, one of the four signal-integrity problems—losses, discontinuities, skew, and crosstalk—can prevent acceptable performance. The first step is being aware of these problems. The second step is to identify their root causes and to develop design guidelines that enable navigation through the minefield. A software-simulation tool that can model signal-interconnect interaction and account for each of the four effects is an essential tool with which to gain confidence in a design before committing to hardware. The combination of best design practices, new materials, new technologies, and analysis tools can dramatically increase the number of successful high-speed-serial-link designs.EDN

AUTHORS' BIOGRAPHIES

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DESIGN NOTES

Supercapacitors Can Replace a Backup Battery for Power Ride-Through Applications – Design Note 450

Jim Drew

Introduction

Supercapacitors (or ultracapacitors) are finding their way into an increasing number of applications for short-term energy storage and applications that require intermittent high energy pulses. One such application is a power ride-through circuit, in which a backup energy source cuts in and powers the load if the main power supply fails for a short time. This type of application has typically been dominated by batteries, but electric double layer capacitors (EDLCs) are fast making inroads as their price-per-farad, size and effective series resistance per capacitance (ESR/C) continue to decrease.

Figure 1 shows a 5V power ride-through application where two series-connected 10F, 2.7V supercapacitors charged to 4.8V can support 20W for over a second. The LTC3225, a new charge-pump-based supercapacitor charger, is used to charge the supercapacitors at 150mA and maintain cell balancing while the LTC4412 provides automatic switchover between the supercapacitor and the main supply. The LTM4616 dual output DC/DC µModule™ regulator creates the 1.8V and 1.2V outputs. With a 20W load, the output voltages remain in regulation for 1.42 seconds after the main power is removed.

Supercapacitor Characteristics

A 10F, 2.7V supercapacitor is available in a 10mm × 30mm 2-terminal radial can with an ESR of 25mΩ. One advantage supercapacitors offer over batteries is their long lifetime. A capacitor's cycle life is quoted as greater than 500,000 cycles, whereas batteries are specified for only a few hundred cycles. This makes the supercapacitor an ideal "set and forget" device, requiring little or no maintenance.

Two critical parameters of a supercapacitor in any application are cell voltage and initial leakage current. Initial leakage current is really dielectric absorption current, which disappears after some time. The manufacturers of supercapacitors rate their leakage current after 100 hours of applied voltage while the initial leakage current in those first 100 hours may be as much as 50 times the specified leakage current.

The voltage across the capacitor has a significant effect on its operating life. When used in series, the supercapacitors must have balanced cell voltages to prevent overcharging of one of the series capacitors. Passive cell

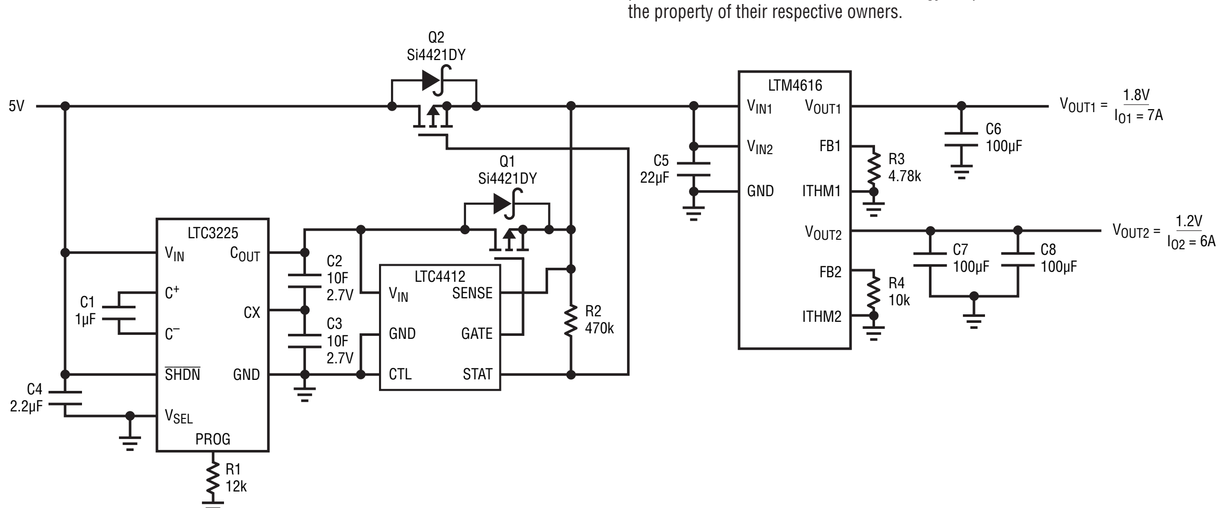

Figure 1. 5V Ride-Through Application Circuit Delivers 20W for 1.42 seconds

balancing, where a resistor is placed across the capacitor, is a popular and simple technique. The disadvantage of this technique is that the capacitor discharges through the balancing resistor when the charging circuit is disabled. The rule of thumb for this scheme is to set the balancing resistor to 50 times the worst case leakage current, estimated at 2μA/Farad. Given these parameters, a 10F, 2.5V supercapacitor would require a 2.5k balancing resistor. This resistor would drain 1mA of current from the supercapacitor when the charging circuit is disabled.

A better alternative is to use a non-dissipative active cell balancing circuit, such as the LTC3225, to maintain cell voltage. The LTC3225 presents less than 4μA of load to the supercapacitor when in shutdown mode and less than 1μA when input power is removed. The LTC3225 features a programmable charging current of up to 150mA, charging two series supercapacitors to either 4.8V or 5.3V while balancing the individual capacitor voltages.

To provide a constant voltage to the load, a DC/DC converter is required between the load and the supercapacitor. As the voltage across the supercapacitor decreases, the current drawn by the DC/DC converter increases to maintain constant power to the load. The DC/DC converter drops out of regulation when its input voltage reaches the minimum operating voltage (V_{UV}).

To estimate the requirements for the supercapacitor, the effective circuit resistance (R_T) needs to be determined. R_T is the sum of the capacitors' ESRs plus the circuit distribution resistances, as follows:

$$R_T = ESR + R_{DIST}$$

Assuming 10% of the input power is lost in the effective circuit resistance when the DC/DC converter is at the minimum operating voltage, the worst case R_T is:

$$R_{T(MAX)} = \frac{0.1 \bullet V_{UV}^2}{P_{IN}}$$

The voltage required across the supercapacitor at the minimum operating voltage of the DC/DC converter is:

$$V_{C(UV)} = \frac{V_{UV}^2 + P_{IN} \bullet R_T}{V_{UV}}$$

The required effective capacitance can then be calculated based on the required ride-through time (T_{RT}), and the initial voltage on the capacitor ($V_{C(0)}$) and $V_{C(UV)}$ shown by:

$$C_{EFF} = \frac{2 \bullet P_{IN} \bullet T_{RT}}{V_{C(0)}^2 - V_{C(UV)}^2}$$

The effective capacitance of a series-connected bank of capacitors is the effective capacitance of a single capacitor divided by the number of capacitors while the total ESR is the sum of all the series ESRs.

The ESR of a supercapacitor decreases with increasing frequency. Manufacturers usually specify the ESR at 1kHz, while some manufacturers publish both the value at DC and at 1kHz. The capacitance of supercapacitors also decreases as frequency increases and is usually specified at DC. The capacitance at 1kHz is about 10% of the value at DC. When using a supercapacitor in a ride-through application where the power is being sourced for seconds to minutes, use the effective capacitance and ESR measurements at a low frequency, such at 0.3Hz. Figure 2 shows the ESR effect manifested as a 180mV drop in voltage when input power is removed.

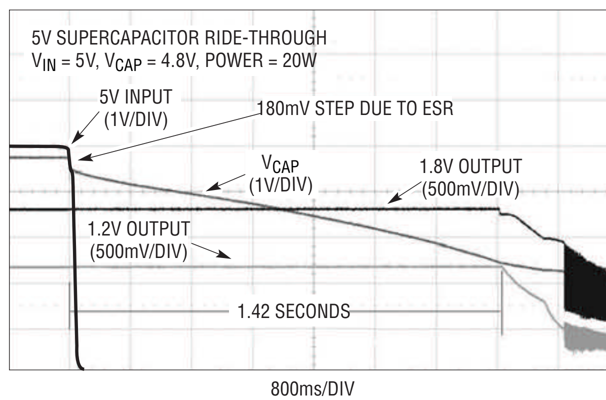

Figure 2. 5V Ride-Through Application Timing

Conclusion

Supercapacitors can meet the needs of power ride-through applications where the time requirements are in the seconds to minutes range. Supercapacitors offer long life, low maintenance, light weight and environmentally friendly solutions when compared to batteries. To this end, the LTC3225 provides a compact, low noise solution for charging and cell balancing series-connected supercapacitors, without degrading performance.

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Add margining capability to a dc/dc converter

Brian Vasquez, Maxim Integrated Products, Dallas, TX

You can easily add margining capability—that is, the ability to digitally adjust the output voltage—to a dc/dc converter by making a single connection to the circuit (**Figure 1**). The dashed line in the **figure** shows the connection. The extra IC is a two- or four-channel, I^2C (inter-integrated-circuit)-adjustable-current DS4402 or DS4404 DAC. Because each DAC output is 0 mA at power-up, the extra circuitry is essentially transparent to the system until you write a command using the I^2C bus.

For example, assume that the input voltage is 3 to 5.5V; the output voltage is 1.8V, which is the desired nominal output voltage; and the feedback voltage is 0.6V. You can obtain the feedback voltage from the dc/dc converter's data sheet; be sure to verify that it is within the output-voltage range that the current DAC's data sheet specifies as sinking or sourcing voltage depending on whether you are sinking or sourcing current. You should also verify the input impedance of the dc/dc converter's feedback pin. The circuit in **Figure 1** assumes a high impedance.

Assume that you want to add a ±20% margining capability to the dc/dc converter's output so that the maximum, nominal, and minimum output voltages would be 2.16, 1.8, and 1.44V, respectively. First, determine the necessary relationship between R_1 and R_2, which yields the nominal output when the current of the DS4404 DAC is 0 mA:

$$V_{FB} = V_{OUTNOM}\left(\frac{R_2}{R_2+R_1}\right), \quad (1)$$

where V_{FB} is the feedback voltage and V_{OUTNOM} is the nominal output voltage. Solving for R_1,

$$R_1 = R_2\left(\frac{V_{OUTNOM}}{V_{FB}}-1\right). \quad (2)$$

For this example,

$$R_1 = R_2\left(\frac{1.8V}{0.6V}-1\right)=2\times R_2. \quad (3)$$

Summing the currents at the feedback node derives the current to make the output voltage increase to the maximum output voltage:

$$I_{R1} = I_{R2} + I_{DS4404}, \quad (4)$$

where I_{R1} is the current through R_1, I_{R2} is the current through R_2, and I_{DS4404} is the current into the DAC.

$$I_{DS4404} = I_{R1} - I_{R2}. \quad (5)$$

$$I_{R1} = \left(\frac{V_{OUTMAX}-V_{FB}}{R_1}\right); I_{R2} = \left(\frac{V_{FB}}{R_2}\right), \quad (6)$$

where V_{OUTMAX} is the maximum output voltage.

$$I_{DS4404} = \left(\frac{V_{OUTMAX}-V_{FB}}{R_1}\right)-\left(\frac{V_{FB}}{R_2}\right). \quad (7)$$

You can simplify **Equation 7** by solving **Equation 1** for R_2 and then substituting, which yields:

$$I_{DS4404} = \frac{V_{OUTMAX}-V_{OUTNOM}}{R_1}. \quad (8)$$

In margin percentage, you can express **Equation 8** as:

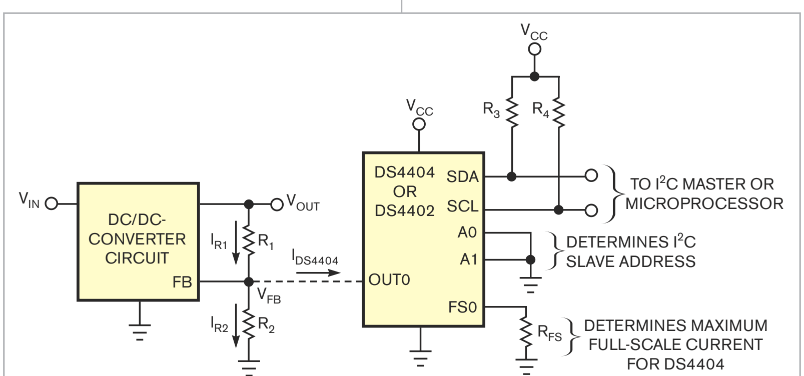

Figure 1 The circuitry to the right of the dashed line adds margining capability.

DIs Inside

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$$I_{DS4404} = \frac{V_{OUTNOM} \times MARGIN}{R_1}, \quad (9)$$

where the margin is 0.2 to implement ±20% margining in this case. Before you can use this relationship to calculate R_1 and R_2, you must select the full-scale current.

According to the DS4404's data sheet, the full-scale current must be 0.5 to 2 mA to guarantee the specifications for accuracy and linearity. Unfortunately, no formula is available for calculating the ideal full-scale current. The desired number of steps, the step size, and the values for R_1 and R_2 influence that value. Another factor affecting the full-scale current value is whether there is a requirement that a particular register setting corresponds to a particular margin percentage.

In any case, your selection of a full-scale current will likely require several iterations, in which you select an arbitrary value within the range and then calculate R_1, R_2, R_{FS} (full-scale resistance), and step size. When you've determined an acceptable full-scale-current value, you may want to further adjust it or some of the resistor values to ensure that the resistor values you finally specify are commonly available.

To calculate R_1 for the original example, make the full-scale current equal to the current of the DS4404. This step gives you 31 equal increments, or steps, from the nominal output voltage to the maximum output voltage, as well as 31 steps from the nominal output voltage to the minimum output voltage. This resolution is more than adequate for this example.

You could, for instance, begin by arbitrarily choosing the full-scale current in the center, or 1.25 mA, of the specified range and then performing all the calculations. Instead, for illustrative purposes, the calculations are shown for the endpoints of the range: 0.5 and 2 mA. Analyzing the 0.5-mA case first, you perform the following calculations and then repeat for the 2-mA case.

Using **Equation 9** and solving for R_1 yields:

$$R_1 = \frac{V_{OUTNOM} \times MARGIN}{I_{DS4404}} = \frac{1.8 \times 0.2}{0.5 \times 10^{-3}} = 720\Omega. \quad (10)$$

$$R_2 = \frac{R_1}{2} = \frac{720}{2} = 360\Omega. \quad (11)$$

To calculate the full-scale resistance, use the formula and the reference voltage in the DS4404's data sheet:

$$R_{FS} = \frac{V_{REF}}{I_{FS}} \times \frac{31}{4} = \frac{1.23}{0.5 \times 10^{-3}} \times \frac{31}{4} = 19{,}065\Omega \approx 19\ k\Omega. \quad (12)$$

$$STEP\ SIZE = \frac{I_{FS}}{NO.\ OF\ STEPS} = \frac{0.5 \times 10^{-3}}{31} = 16.1\ \mu A/STEP, \quad (13)$$

where R_{FS} is the full-scale resistance, V_{REF} is the reference voltage, and I_{FS} is the full-scale current.

Finally, for completeness, you determine the DS4404's output current as a function of register setting:

$$I_{OUT}(REGISTER\ SETTING) = STEP\ SIZE \times REGISTER\ SETTING. \quad (14)$$

Note that this register setting does not include the sign bit, which selects sink or source. The DS4404 sinks current when the sign bit is zero, making the output voltage increase to the maximum output voltage. It sources current when the sign bit is one, making the output voltage decrease toward the minimum output voltage.

Now, you can repeat the calculations for the 2-mA case.

$$R_1 = \frac{V_{OUTNOM} \times MARGIN}{I_{DS4404}} = \frac{1.8 \times 0.2}{2 \times 10^{-3}} = 180\Omega. \quad (15)$$

$$R_2 = \frac{R_1}{2} = \frac{180}{2} = 90\Omega. \quad (16)$$

$$R_{FS} = \frac{V_{REF}}{I_{FS}} \times \frac{31}{4} = \frac{1.23}{2 \times 10^{-3}} \times \frac{31}{4} = 4766\Omega \approx 4.7\ k\Omega. \quad (17)$$

$$STEP\ SIZE = \frac{I_{FS}}{NO.\ OF\ STEPS} = \frac{2 \times 10^{-3}}{31} = 64.5\ \mu A/STEP. \quad (18)$$

Comparing R_1 and R_2 for the two cases—with a full-scale current of 0.5 or 2 mA—0.5 mA is the more attractive value because the resistances are higher. **EDN**

A better approach to designing an RTD interface with a spreadsheet

Aubrey Kagan, Emphatec, Markham, ON, Canada

An earlier Design Idea described how to linearize the output of an RTD (resistance-temperature-detector) sensor and how to calculate the resistor values using a spreadsheet (**Reference 1**). That idea limited the use of Microsoft (www.microsoft.com) Excel to calculating the coefficients you need for the polynomial expression and stopped short of using Excel to calculate the resistor values. You can generalize this proposed approach such that you can select any type of RTD and any temperature range, but this Design Idea limits the details to the following example.

You can download the worksheet (**Figure 1**) from the Web version of this Design Idea at www.edn.com/080918di1. You plot the chart as an XY diagram, and you create the trend line on the chart using a second-order polynomial, which will appear on the chart. The original Design Idea included this information. Unfortunately, you cannot access the coefficients you generate in this way from the worksheet, so you cannot directly calculate the resistor values.

To access the polynomial coefficients, you can use Excel's LINEST

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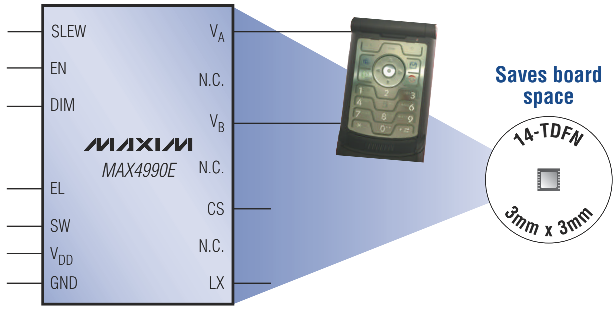

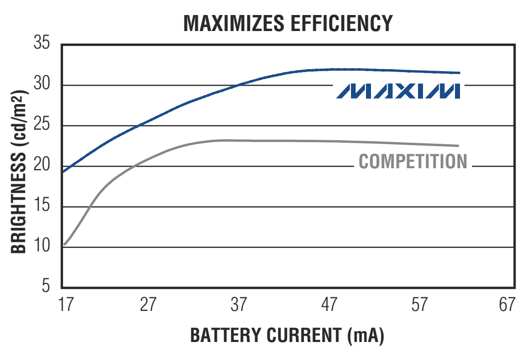

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Maximizes efficiency

- High brightness (250V_{P-P}, max) with low current consumption
- 40% brighter than the competition

Part	Input-Voltage Range (V)	Peak-to-Peak Output Voltage (V, max)	ESD Protection (kV)	Features	Package (mm x mm)	Price† ($)
MAX4990E	2.4 to 5.5	250	±15	Soft turn-on/off, slew-rate control	14-TDFN (3 x 3)	0.99

*Human Body Model.

†1000-up recommended resale. Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates. Not all packages are offered in 1k increments, and some may require minimum order quantities.

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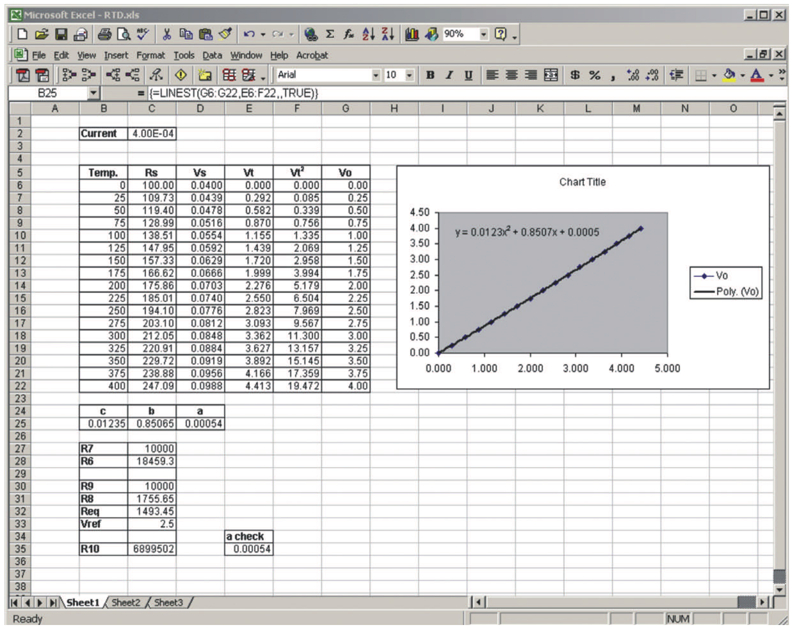
array formula. It prescribes a specific way of entering data; without that protocol, Excel will not provide the desired results. LINEST returns a number of regression statistics; to allow for these statistics, you must first highlight the range on the worksheet on which you want the regression results. Only the polynomial coefficients are important in this example, so this Design Idea limits the returned results by selecting block B24:D24 for those three values. You then enter the following line into the formula bar at the top of the worksheet: =LINEST(G5:G21,E5:F21,,TRUE).

Simultaneously press the Control, Shift, and Enter keys rather than just Enter to terminate this command. The coefficients will then drop into the selected range. Excel will add the braces, { }, to indicate the array formula. The input range of the function in the formula above includes the Vt^2 column, allowing LINEST to create a second-order polynomial equation.

You can enter user-selected values as set numbers, providing easy and quick modification and an immediate update of the calculated values. These values include the current source through the RTD, the reference voltage, and the value of R_7 and R_9, all of which are "named" cells that the formulas refer to. The idea rewrites the original formulas to isolate the desired variable. You will find each in the associated cells for R_6, R_8, and R_{10} on the worksheet. You could also complete the model by creating an automatic look-up of standard resistor values (**Reference 2**).EDN



Current	4.00E-04

Temp.	Rs	Vs	Vt	Vt^2	Vo
0	100.00	0.0400	0.000	0.000	0.00
25	109.73	0.0439	0.292	0.085	0.25
50	119.40	0.0478	0.582	0.339	0.50
75	128.99	0.0516	0.870	0.756	0.75
100	138.51	0.0554	1.155	1.335	1.00
125	147.95	0.0592	1.439	2.069	1.25
150	157.33	0.0629	1.720	2.958	1.50
175	166.62	0.0666	1.999	3.994	1.75
200	175.86	0.0703	2.276	5.179	2.00
225	185.01	0.0740	2.550	6.504	2.25
250	194.10	0.0776	2.823	7.969	2.50
275	203.10	0.0812	3.093	9.567	2.75
300	212.05	0.0848	3.362	11.300	3.00
325	220.91	0.0884	3.627	13.157	3.25
350	229.72	0.0919	3.892	15.145	3.50
375	238.88	0.0956	4.166	17.359	3.75
400	247.09	0.0988	4.413	19.472	4.00

c	b	a
0.01235	0.85065	0.00054

R7	10000
R6	18459.3
R9	10000
R8	1755.65
Req	1493.45
Vref	2.5
R10	6899502

a check
0.00054

Figure 1 The linearizing values of an RTD circuit accompany a graph of the output voltage.

REFERENCES

1. Villanucci, Robert S, "Design an RTD interface with a spreadsheet," *EDN*, Feb 7, 2008, pg 57, www.edn.com/article/CA6526816.
2. Kagan, Aubrey, *Excel by Example: A Microsoft Excel Cookbook for Electronics Engineers*, Elsevier/Newnes, May 2004, ISBN 0750677562.

Shunt regulator monitors battery voltage

Vladimir Rentyuk, Modul-98 Ltd, Zaporozhye, Ukraine

A TL431 shunt regulator is a perfect choice for many applications. You can use it as a comparator with hysteresis by taking advantage of its inner voltage reference along with few additional components. You can use this comparator with hysteresis, like a Schmitt trigger, as a simple battery monitor (**Figure 1**). You calculate the threshold voltage, V_{T+}, of this comparator as $V_{T+}=V_{REF}\times(1+R_1/R_3)$, where V_{REF}, the internal reference voltage of shunt-regulator TL431, is 2.5V.

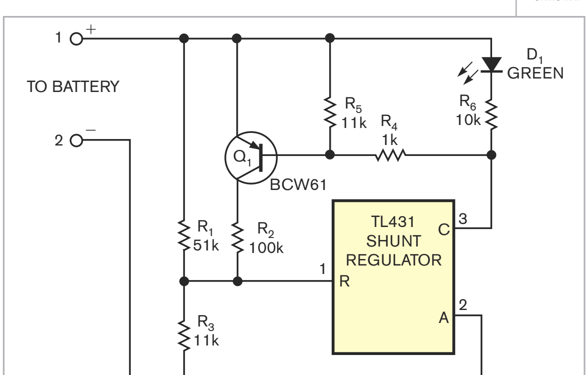
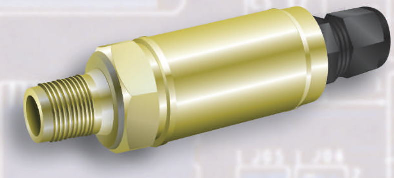


Figure 1 A shunt regulator and associated circuitry function as a Schmitt trigger, lighting LED_1 when the battery is fully charged.

When the battery voltage is higher than the threshold voltage, the cathode voltage of the TL431 is at its low level of approximately 2V, and transistor Q_1 turns on, lighting LED_1. You calculate the release voltage, V_{T-}, of the trigger as $V_{T-}=V_{REF}\times(1+R_1\times R_2/(R_1+R_2)\times 1/R_3)$.

When the battery voltage is less than the release voltage, the cathode voltage of the TL431 goes to its high level—to the battery voltage. Transistor Q_1 turns off, and LED_1 does not shine. LED_1 turns on again when the battery voltage, after recharging, exceeds the threshold voltage.EDN



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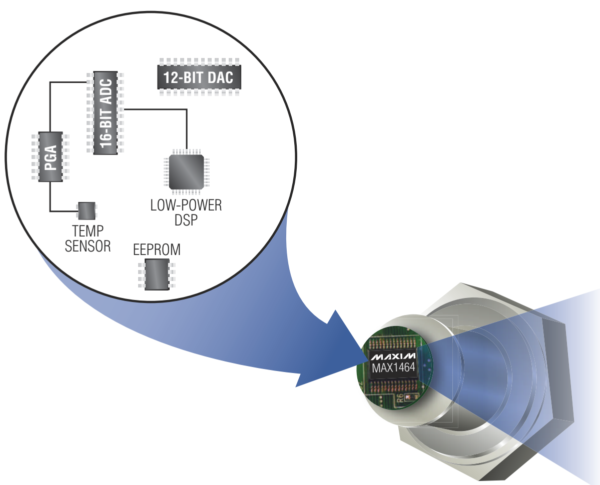

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MAX1452	2.0/2.5	-40 to +125	16	2.95
MAX1455	3.0/6.0		33	3.25
MAX1464	2.5/3.2**		82	4.80

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Power supply meets automotive-transient-voltage specs

Francesc Casanellas, Aiguafreda, Spain

Figure 1 shows a power supply that delivers 5V from a 12V battery. With only a few components, the supply copes with all the automotive transients that ISO (International Organization for Standardization) 7637-1 lists without the need for a bulky transient-voltage suppressor. In normal operation, R_3 connects to the common through a microcontroller port. In standby mode, R_3 stays open, and the quiescent current of the supply decreases from approximately 2.8 mA to approximately 160 μA, and the output voltage then drops to approximately 3.5V. If your application doesn't require a standby mode, suppress R_3 and set R_5 to 220Ω. With most common zener diodes, you would then set R_5 to 120Ω and D_1 to 4.3V. You can use the circuit in 24V systems if D_2 is 36V.

If the voltage increases, the current through D_1 and the base of Q_3 increases, so Q_3 increases the current of Q_2, which lowers the gate-to-source voltage of Q_1. If the input voltage surpasses 19V, D_2 starts to conduct and makes Q_2 switch off Q_1, so permanent overvoltages as high as 200V cannot damage the circuit. The Miller capacitance of Q_1 makes it act as a fast integrator, which keeps the system stable. If you remove D_2, you must replace Q_3 with a high-voltage transistor, such as an MMBTA42.

If you omit D_2, the circuit cannot withstand permanent overvoltages without Q_1's overheating. In this case, however, the circuit can cope with all the impulses, including the load-dump pulse, of ISO 7637-1. You should remove D_2 only if C_1 cannot maintain the voltage during long overvoltages, such as the load-dump pulse, and keeping the voltage is critical.

An added advantage of this circuit over most IC-voltage regulators is that it can sink current through D_1 and Q_3. This feature allows the use of diodes to fully protect the microprocessor's inputs. Soldering the D-Pack package to a couple of 1-cm^2 copper pads allows the circuit to source 300 mA at 10 to 16V or 150 mA at 20 to 32V. More dissipation area allows for higher currents.EDN

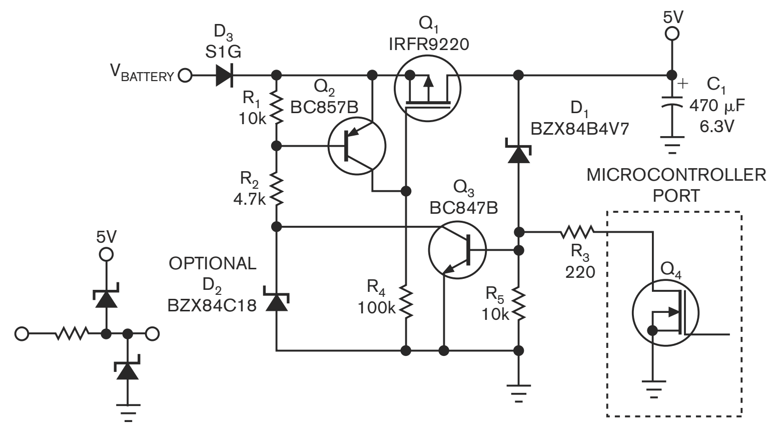


Figure 1 This automotive regulator withstands overvoltages that ISO 7637-1 specifies.

Locked-sync sine generator covers three decades with low distortion

Alfredo H Saab and Tina Alikahi, Maxim Integrated Products, Sunnyvale, CA

Analog applications, such as testing, calibration, and general system operation, often require a sine waveform of accurate amplitude and frequency, with low THD (total harmonic distortion). Some applications demand that the generator of such waveforms have the ability to accurately synchronize the output with an external timing signal. Simple sine-wave generators can offer various degrees of this performance, but maintaining low THD with constant amplitude is a problem, particularly if the output and the synchronization signal must remain locked through an extended range of frequencies.

The circuit in **Figure 1** can synchronize a sine-wave output through three decades of frequency—20 Hz to 20 kHz—and maintain low THD and constant amplitude (**Table 1**). The synchronizer IC, an NXP Semiconductors (www.nxp.com) 74HC4046, is a PLL (phase-locked loop) with a VCO (voltage-controlled oscillator) and a phase/frequency detector. It has three internal phase detectors, but this design uses the one with a frequency-capture range equal to that of the VCO-frequency range (the maximum frequency minus the minimum frequency).

The circuit's general-purpose binary frequency divider, the 74HC4060, connects between the VCO output and the 74HC4046 feedback (phase/frequency-comparator) input and has a division ratio of 64. When the PLL is locked, therefore, the Q6 output of the 74HC4060 generates a square wave equal to 1/64th of the VCO-output frequency. The components that determine the 74HC4046 center frequency, C_1 and R_1, determine the VCO-frequency range from 20×64 to 20,000×64 from the minimum to the maximum level of the VCO's input-voltage range.

A switched-capacitor lowpass filter, the Maxim (www.maxim-ic.com) MAX297, whose cut-off frequency by design equals 1/50th of the clock frequency you apply to it, has for signal input the same square wave it uses for the PLL feedback, and its clock input attaches to the VCO output. Because the clock and signal inputs always have a frequency ratio of 64, the input signal always falls within the filter bandpass. No input harmonics fall within this bandpass because the ratio of the clock frequency to frequency is less than 50 for all of them. (For the lowest second harmonic, the ratio is 32.) The THD, up to the 32nd harmonic, is lower than 0.1%.

The fact that the filter's input signal is a square wave with a 50% duty cycle helps in this application because a square wave contains only odd harmonics of the fundamental, and the lowest-frequency harmonic is the third, which is well within the filter's deep-attenuation range.

You can frequency-modulate the synchronization signal, but that task entails a compromise between the synchronization-tracking speed (or maximum modulation frequency and depth) and the frequency-locking range, which the PLL's lowpass filter components, R_2, R_3, and C_2, set. Modulation speed is limited for the values the **figure** shows because those values are optimized for an extended-frequency locking range. You can download more information, including a full data sheet for the MAX297, from www.maxim-ic.com (**Reference 1**).EDN

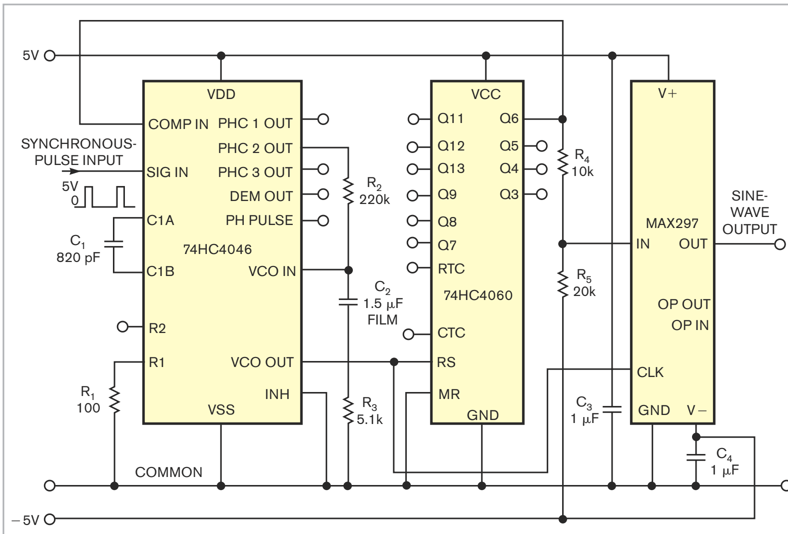


Figure 1 This three-IC sine-wave generator covers three frequency decades, provides low distortion, and allows you to synchronize it with an external signal.

REFERENCE

1 "MAX293/MAX294/MAX297 8th-Order, Lowpass, Elliptic, Switched-Capacitor Filters, Revision 2," June 2008, Maxim, http://datasheets.maxim-ic.com/en/ds/MAX293-MAX297.pdf.

TABLE 1 AMPLITUDE VERSUS FREQUENCY

Frequency (Hz)	Amplitude (V rms)
20	1.470
50	1.472
100	1.472
200	1.473
500	1.473
1000	1.473
2000	1.472
5000	1.473
10,000	1.473
20,000	1.472

Gaining design-chain traction

Avnet Inc (www.avnet.com) continues to use demand creation—the use of distributor-supplied suites of engineering services to encourage product training and guidance—as an active tool in weathering the stormy economy. "The market continues to be a difficult one, but we are starting to really gain some significant traction in a focus we've really been pushing in the last couple of years, which is trying to move a bit up the value chain," says Harley Feldberg (**photo**), president of Avnet EM (Electronics Marketing). Feldberg says that Avnet is still a significant, active fulfillment-components distributor but believes that the company has become a leader in demand creation, or what Avnet internally calls "design chain."

"Demand creation tends to afford you a higher gross margin and a better return. Now, it does require a higher investment because of technical resources and training, but our belief has been for the last couple of years that focusing in that area will help insulate us from these kinds of difficult environments," he says, pointing to Avnet's June quarter, which saw total revenue of $4.68 billion increase 10.4% year over year. Avnet EM sales of $2.73 billion increased 10.8% over the June 2007 quarter.

Avnet noticeably turned up its focus on demand creation after its 2005 acquisition of Memec. Much of the reason demand creation is gaining traction in today's market, according to Feldberg, has to do with volume OEMs (original-equipment manufacturers). "The volume OEMs that drive so much of the global TAM [total available market] ... much of that volume and much of that design is [directly] handled by our suppliers. As that business has moderated, over the last year especially, there has been significantly increased interest on behalf of many of our suppliers to accelerate their efforts and energy into the next year and the mass market. That [acceleration] really leads them back to distribution. Our ability to represent them for their technologies to win design in that mass market is really a big, big part of our success," says Feldberg.

GREEN UPDATE

INDUSTRY NOT PREPARED FOR REACH

According to recent data from the IPC (www.IPC.org), the electronics supply chain is not prepared for the EU REACH (European Union Registration, Evaluation, Authorization and Restriction of Chemicals) regulation that took effect on June 1, 2007. A survey conducted by the industry group on REACH preparedness in the North American and European interconnect industry found that more than 40% of manufacturing and purchasing personnel do not understand the regulation as it affects their companies. The same holds true for nearly one-third of senior management; 29% of engineering personnel; and 28% of environment, health, and safety personnel.

"REACH will have a far-reaching effect on any company that buys, sells, or uses chemicals," says Tony Hilvers, vice president of industry programs for IPC. "And that pretty much sums up the entire electronics supply chain. The survey clearly indicates that our industry is woefully unprepared for the hit it's about to take."

IPC's electronic survey shows that only 18.3% of company respondents have identified or inventoried all substances in their products. Moreover, only 60.5% of chemical supplier respondents are planning to register or preregister substances at all.

To comment on this topic, visit www.edn.com/blog/690000269/post/1850030785.html.

OUTLOOK

CONTRACT MANUFACTURING SHRINKS

The electronics CM (contract-manufacturing) industry is undergoing a transformation, according to iSuppli Corp (www.isuppli.com). The CM industry, made up of EMS (electronics-manufacturing-services) and ODM (original-design-manufacturing) providers, is set to see revenue expand to $432.3 billion by 2012, rising at a CAGR (compound-annual-growth rate) of 7.2% from 2007. The $126.7 billion gain represents a slowdown compared with the 15.5% CAGR CM revenue enjoyed from 2002 to 2007 and the 49% CAGR of the 1990s.

"Several factors are inhibiting the revenue surge of the past 20 years," says Adam Pick, principal analyst, EMS/ODM at iSuppli. "Those factors include the statistical law of large numbers, which makes it difficult for such a large market to expand much on a percentage basis."

Pick cautions that a major consequence of this slower growth is continued consolidation among the world's top CM providers. "As many of the larger CMs attempt to retrench and 'right-size' their businesses, revenue growth has become stagnant or even negative." Therefore, he says, "an examination of possible acquisition targets becomes a top priority for larger companies."

productroundup

SENSORS AND TRANSDUCERS

3-D-orientation sensor uses click/double-click detection

Using MEMS technology, the FC30 sensor embeds 3-D-orientation functions and click/double-click detection, allowing integration of mouse-button controls. The device's three external interrupt lines allow developers to build automatic-portrait/landscape-recognition applications. Available in a 3×5×0.9-mm LGA-14 package, the FC30 sensor costs $1 (high volumes).
STMicroelectronics, www.st.com

Microcontroller family features OTG functions

The vendor's 12-member PIC24-FJ256GB1 16-bit USB microcontroller family features 100-nA standby current, 256 kbytes of flash memory, and 16 kbytes of RAM. The integrated USB 2.0 device provides embedded-host, dual-role, and OTG (On-The-Go) functions. The devices allow the addition of advanced USB features to embedded designs. Integrating the CTMU (charge-time-measurement-unit) peripheral and the royalty-free mTouch Sensing Solution software-development kit, the microcontrollers enable designers to add a capacitive-touch user interface without using external components. The microcontroller family is available in TQFP-64, -80, or -100 packages, and prices start at $3.47 (10,000).
Microchip Technology, www.microchip.com

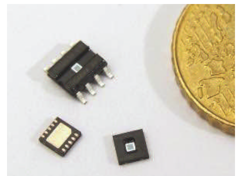
Ambient-light photo sensor controls display backlighting

Approximating the spectral-response curve of the human eye, the miniature, surface-mount APDS-9008 ambient-light photo sensor controls display backlighting. The APDS-9008 analog-output photo sensor offers a 1.6 to 5.5V voltage range. Aiming at applications requiring measurement of ambient light for controlling display-backlighting power consumption, the device has a V_{CC} as low as 1.6V. Available in a lead-free, miniature-chip-LED surface-mount package, the APDS-9008 costs 60 cents (2500).

Avago Technologies, www.avagotech.com

Light-to-voltage sensor suits automotive industry

Joining the vendor's Sensor-EyeCTM line, the MLX75305 light-to-voltage sensor suits high-volume automotive, industrial, and consumer applications. Claiming a life span exceeding 15 years, the light sensor's output voltage varies linearly with incident light. The IC integrates the photodiode, a transimpedance amplifier, and a linear-voltage-output stage on the sensor chip. This integration allows stable light responsivity over time and over temperature and improved noise behavior, compared with designs using discrete photodiodes. Meeting AEC-Q100 automotive specifications, the devices provide a −40 to +125°C temperature range; a consumer version of the sensor is also available with an operating temperature as high as 85°C. Available in 3×3×0.65-mm DFN and SO-8 packages, the MLX75305 costs 30 cents (medium quantities).



Melexis, **www.melexis.com**

MEMS-based vibration sensor provides early detection

Based on the vendor's iMEMS motion-signal processing technology, the high-bandwidth ADXL001 MEMS vibration sensor enables monitoring of equipment performance. The industrial vibration and shock sensor allows early detection of motor-bearing vibration and irregularities as high as 22 kHz. Available in dynamic ranges of ±70, ±250, or ±500g, the sensors have a 22-kHz resonant-frequency bandwidth and provide frequency responses to dc. Additional features include a nonlinearity of 0.2% of full-scale range, a −40 to +125°C temperature range, and the ability to function on a 3.3 to 5V supply. The vibration sensor requires no calibration. Measuring 5×5 mm in an LCC-8 ceramic package, the ADXL001 costs $35 (1000).

Analog Devices, **www.analog.com**

productroundup

EMBEDDED SYSTEMS

Conduction-cooled JPEG 2000 PMC card provides real-time compression/decompression

Available in the PMC form factor, the Orion CC dual-channel video-compression/decompression board suits use in VME and CompactPCI systems. The rugged, conduction-cooled board uses dual onboard JPEG 2000 engines, supporting full-frame encoding of standard 625-line PAL or 525-line NTSC composite video. Using an image-coding system and state-of-the-art wavelet-technology-based compression techniques, the board has better bit-rate-compression performance than its JPEG predecessor. The Orion CC board costs $4500.

Curtiss-Wright Controls Embedded Computing, www.cwcembedded.com

High-density, 672-channel T3 PMC suits voice and data applications

The wanPMC-C1T3 WAN PMC adapter terminates 672 HDLC channels. The adapter enables advanced voice and data applications, such as VOIP, video on demand, voice conferencing, and Internet routing. The adapter transfers 64 or 32 bits of data at speeds as high as 66 MHz and conforms to the PCI-local-bus 2.1 specification. It also offers an M13 multiplexer, 28 T1/E1 framers, signal conditioning, B3ZS transmission encoding and receiver decoding, and local and remote loopback. The adapter comes with both Red Hat and Timesys embedded Linux drivers. The WAN PMC sells for $2281.

One Stop Systems, www.onestopsystems.com

Sensors ease integration into drop-in-networking applications or ZigBee networks

The battery-powered, long-life XBee wireless sensors provide easy integration into drop-in-networking applications or ZigBee networks. The sensors allow customers to collect real-time data from multiple nodes across a ZigBee network and target use in building-automation, security, energy-management, food-management, and freight/vehicle-monitoring applications. XBee sensors monitor a combination of temperature and light or a combination of temperature, humidity, and light. The XBee temperature/light and temperature/humidity/light models sell for $125 and $165, respectively.

Digi International, www.digi.com

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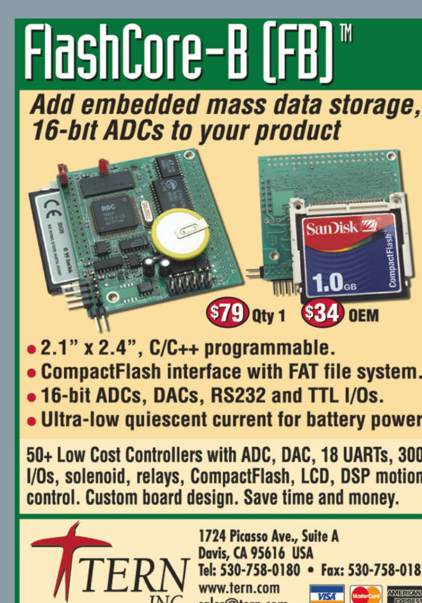
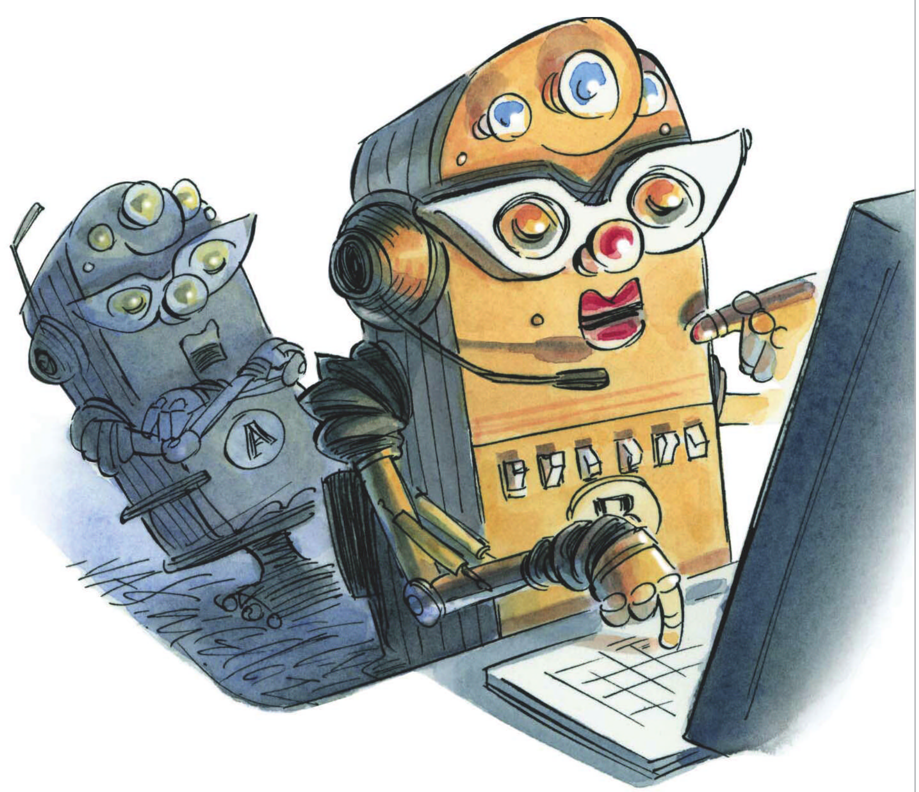


BY CRAIG HERMANN • ENGINEER

Passive part becomes aggressive



DANIEL VASCONCELLOS

In 1981, I landed a job maintaining a computerized telephone-answering service. The system comprised a 16-bit minicomputer, disk drives, a paper-tape reader, a card reader, and a Teletype. The computer had switches and lights on the front panel and external I/O cards for all of the devices. The answering service assisted doctors, ambulances, and other critical-care clients, and the computer had to stay up and running as much as possible. There were two computers, aptly named A and B. One was supposed to be online, and the other was to be ready to go online if the online system failed.

The system ran on a real-time operating system and was very impressive in its time. The computer had 32 kbytes of core memory and four 1-Mbyte disk drives, yet it could route hundreds of phone calls to 16 operators.

The B computer was the online system, and the A computer was the offline system. My colleagues informed me that, although the A system had passed all of the diagnostic tests, it could not run the online system, and the B system could not pass the diagnostic tests but ran the online system fine. I did my own testing and found this situation to be true. I wasn't content to leave it that way, though.

The A system would run the online software for 10 minutes, then become unresponsive. The previous repair people had replaced every card in the A system, and it still failed.

I had to somehow compare the systems to determine differences, and I first looked at the interrupts. I knew that the diagnostic software disabled every interrupt except for the interrupt for the device under test. I also knew that the real-time operating system had good interrupt handlers for the devices it used. The only interrupt left to worry about was a spurious interrupt. The minicomputer had 128 possible interrupts, and the real-time operating system used only 10. I wrote software to count the number of spurious interrupts and found that the offline system had hundreds of spurious interrupts per minute. The online system had thousands of spurious interrupts per minute. The B system was far noisier electrically than the A system and still worked better.

Next, I modified the operating system, a backup copy, to "think" it was online. I forced disk, terminal, and Teletype activity to load the system. After 15 minutes, it went to sleep. I ran that test three more times just to prove that the A system would fail. The next step was to run only the Teletype to see whether the computer would continue to run. The test ran this way for several hours.

I then added one device at a time. The test failed with the addition of the second disk-controller card. This result was confusing because this card passed all of the offline diagnostics. The only part that I had not repeatedly swapped was the backplane card that held the I/O cards.

I found that I could run both disk-controller cards, with some rewiring, in the same backplane. When I did, the system tests ran perfectly. I swapped out the bad backplane.

I then put the A system online and watched it for several hours. It did not fail, and none of the users knew anything had changed. I was finally able to take the B system down for some much needed rest.EDN

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